Bangladesh Govt. & UGC Approved
UNIVERSITY OF GLOBAL VILLAGE (UGV), BARISHAL.
THE FIRST SKILL BASED HI-TECH UNIVERSITY IN BANGLADESH

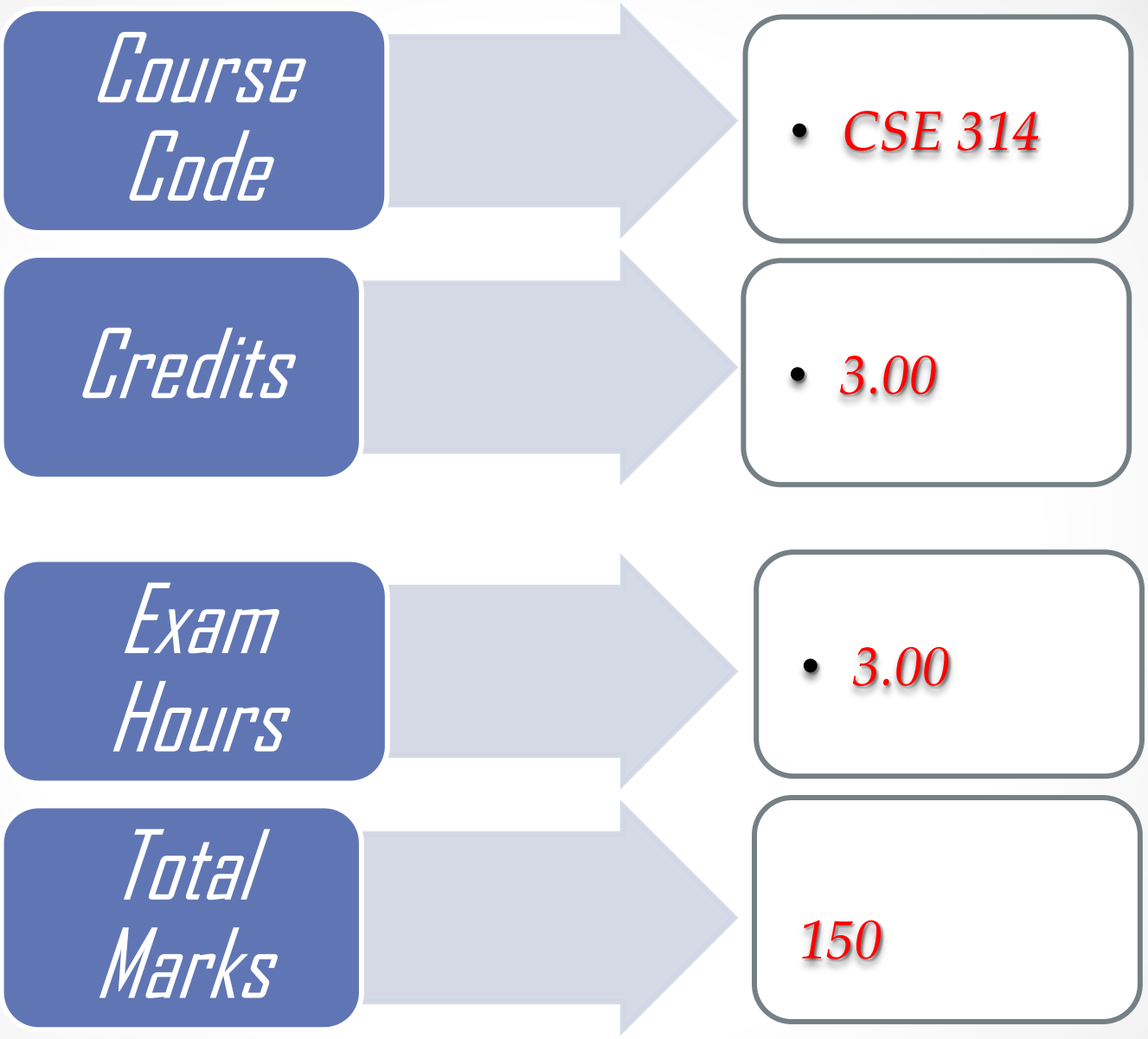
Computer Peripherals And Interfacing

Prepared by:

Md. Abdur Razzak

Asst. Professor.

Department of CSE


Course Code
CSE 314
Credits
3.00
Exam Hours
3.00
Total Marks
150

CLO 1

Understand peripheral devices
Students learn about the different types of peripheral devices, including external and internal devices. They also learn how to connect peripherals to a computer.

CLO 2

- *Understand how peripherals work*
- *Students learn how peripherals work, including how they communicate with the computer's central processing unit.*

CLO 3

- *Understand how to troubleshoot peripherals*
- *Students learn how to troubleshoot common issues with peripherals, such as keyboards, mice, printers, and monitors.*

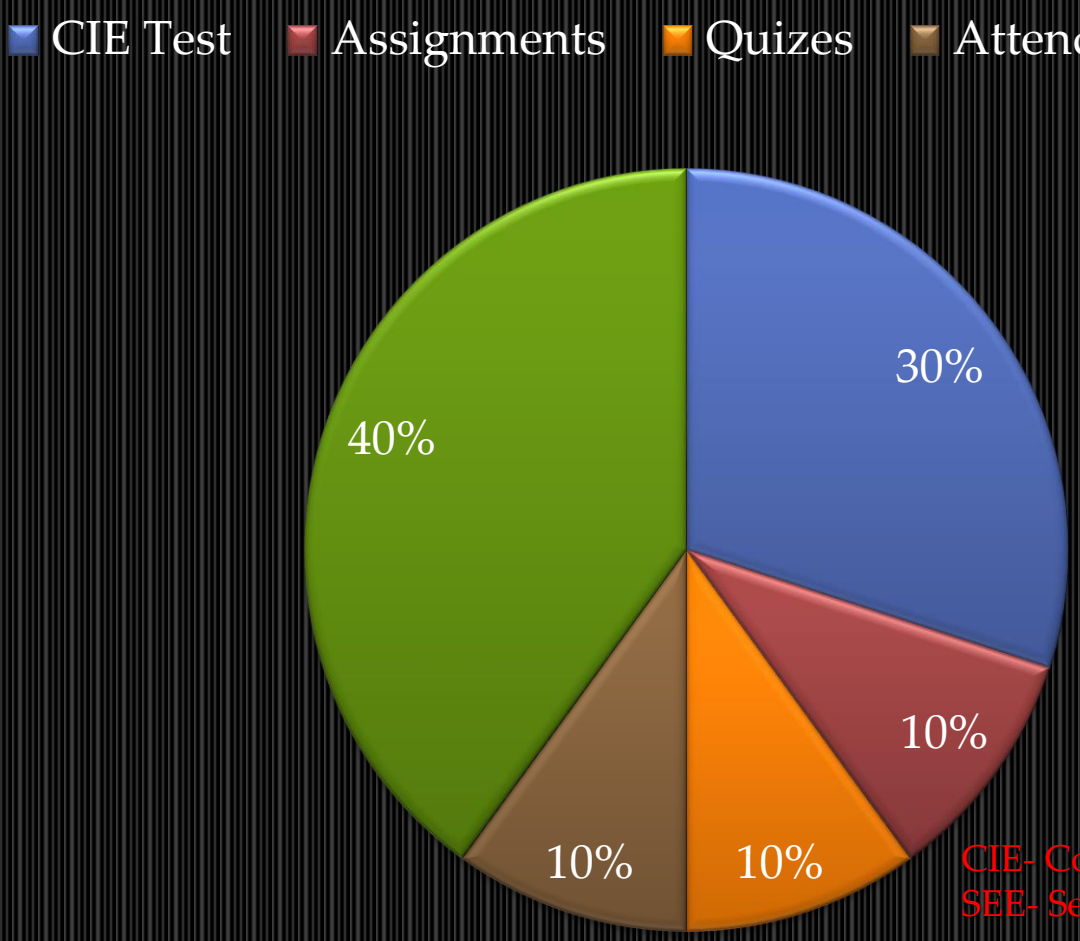
CLO 4

- *Maintain peripherals*
- *Students learn how to maintain peripherals, including how to maintain power supplies, printers, and monitors.*

CLO 5

- *Execute interface of peripherals*
- *Students learn how to interface peripherals with a computer, including how to use ports to connect peripherals.*

Assessment Pattern



CIE- Continues Internal Evaluation
SEE- Semester End Examination

Detailed Assessment Pattern

CIE- Continuous Internal Evaluation (90 Marks)

Bloom's Category Marks (out of 90)	Tests (45)	Assignments (15)	Quizzes (15)	Attendance (15)
Remember	5	03		
Understand	5	04	05	
Apply	15	05	05	
Analyze	10			
Evaluate	5	03	05	
Create	5			

SEE- Semester End Examination (60 Marks)

Bloom's Category	Test
Remember	7
Understand	7
Apply	20
Analyze	15
Evaluate	6
Create	5

Week No	Topic	Teaching Learning Strategy(s)	Assessment Strategy(s)	CLO
1	Introduction to Computer peripherals	Lecture, Reading	Quiz, Assignment	CLO 1
2	Serial And Parallel Transmission-1	Lecture, Reading Assignments	QA, Quiz, Assignment	CLO 1
3	Serial And Parallel Transmission-2	Lecture, Case Studies	Quiz, Assignment	CLO 2
4	INTERRUPTS In Peripherals			CLO 2
5	Interrupt Handler	Lecture, Hands-on Labs	Quiz, Lab Reports	CLO 2
6	Direct Memory Access-1	Lecture, Simulation Exercises	Quiz, Simulation Reports	CLO 1 CLO 2

Week No	Topic	Teaching Learning Strategy(s)	Assessment Strategy(s)	CLO
7	Direct Memory Access-2	Lecture, Reading	Quiz, Assignment	CLO 2
8	Block Data Transfer	Lecture, Reading Assignments	QA, Quiz, Assignment	CLO 2
9	Data Lines	Lecture, Case Studies	Quiz, Assignment	CLO 3
10	Semiconductor Memories and Interfacing-1	Lecture, Hands-on Labs	Quiz, Lab Reports	CLO 3
11	Semiconductor Memories and Interfacing-2	Lecture, Hands-on Labs	Quiz, Lab Reports	CLO 2 CLO 3
12	Semiconductor Memories and Interfacing-3	Lecture, Simulation Exercises	Quiz, Simulation Reports	CLO 3 CLO 4
13	Error detecting and correcting	Lecture, Simulation Exercises	Quiz, Simulation Reports	CLO 3 CLO 4
14	Interfacing with Keyboard	Lecture, Simulation Exercises	Quiz, Simulation Reports	CLO 4
15	**Interfacing Displays**	**Lecture, Simulation Exercises**	**Quiz, Simulation Reports**	CLO 4 CLO 5

16	Interfacing Printer-1	Lecture, Simulation Exercises	Quiz, Simulation Reports	CLO 5
17	Interfacing Printer -2	Lecture, Simulation Exercises	Quiz, Simulation Reports	CLO 4 CLO 5

Week 1

The peripheral devices permit communication of information and storage of information.

Peripherals normally communicate through the CPU.

Some may communicate themselves and memory bypassing CPU

The number and types of peripheral devices depend on the main applications for which the computer system is intended.

COMPONENTS OF A STORED-PROGRAM DIGITAL COMPUTER

- A digital computer executes instructions given to it.
- These instructions first entered into the computer and stored in memory.
- Each location of memory has own address.
- CPU fetch an instruction from memory and executes it.

Instruction: Example

- Load/Store
- Arithmetic/Logical/Shift
- Jump/Branch
- Input/Output

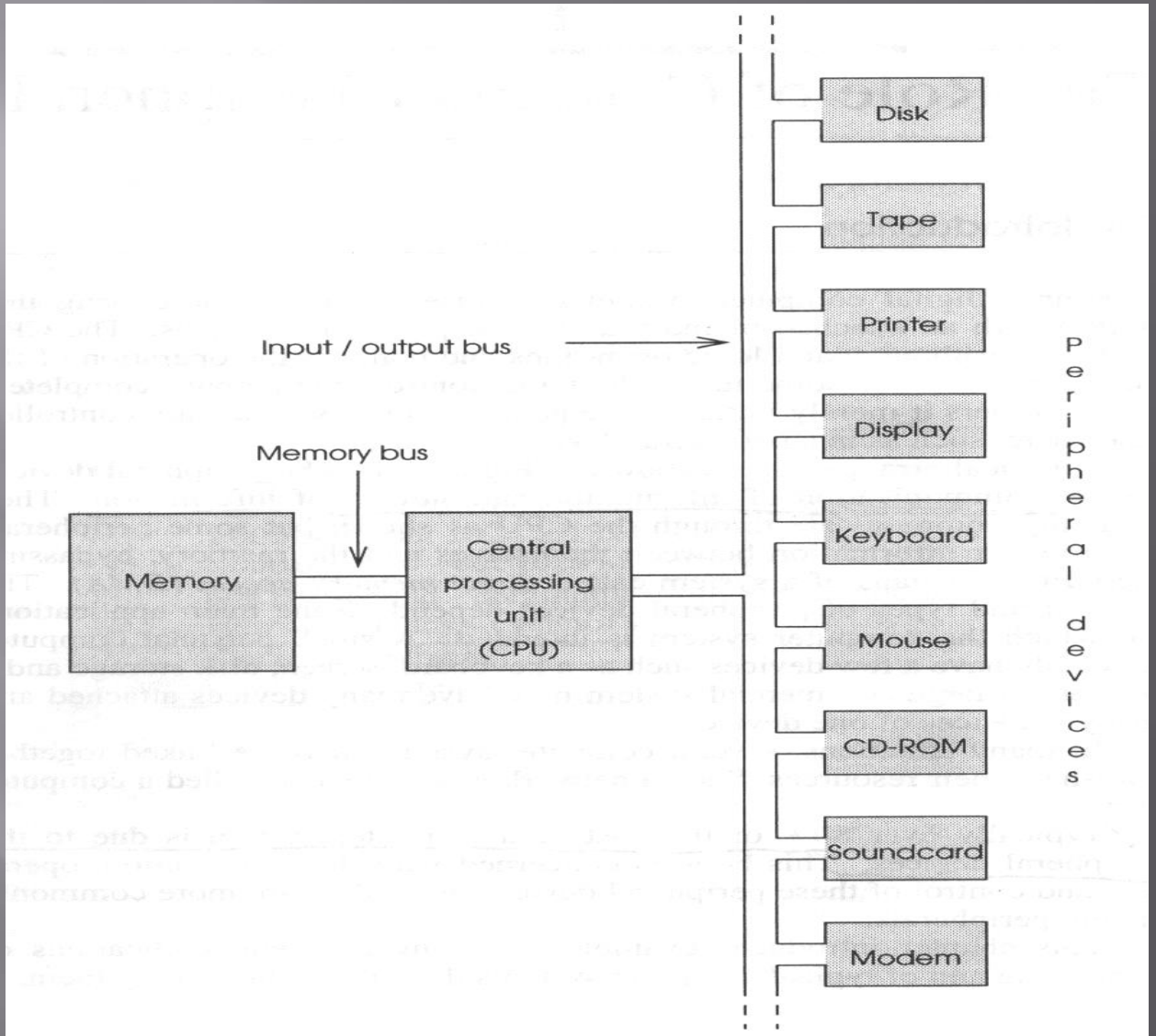


Figure 1.1 *Typical computer system*

Data Highways

- Data (including programs) are moved around the computer on a set of wires forming a data highway (Bus).
- Address Bus, Control Bus, Data Bus

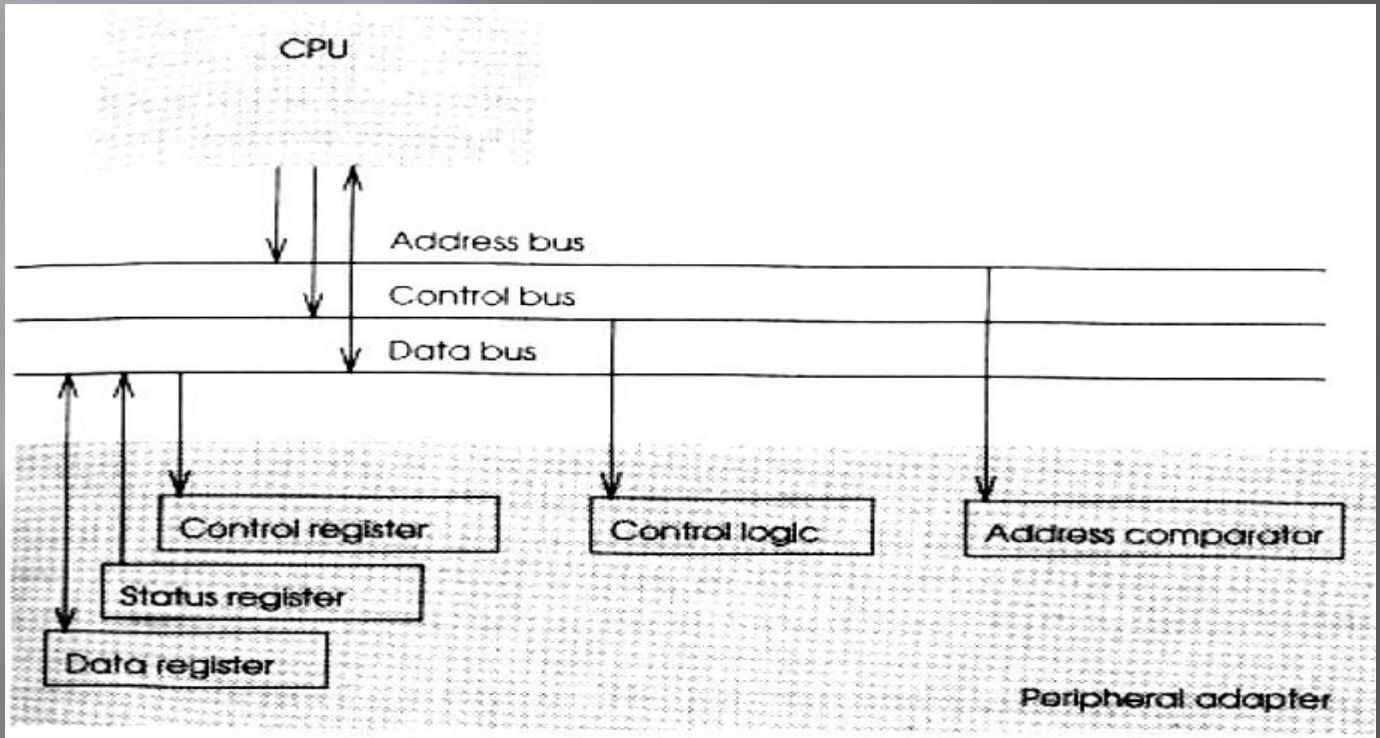


Figure 2.2 *Connection of peripheral adapter to highway*

DATA HIGHWAYS

- ***Data Bus:***
- It contains the information or program instructions required by the CPU.
- The speed of operation of a computer on the rate at which data can be made available and a good way to improve the speed is to add more data lines to transfer more data at a time.
- Small systems use 8-bit data bus.They are relatively slow but of low cost.
- 8086 uses 16-bit and 80386 uses 32-bit bus.

Data Highways

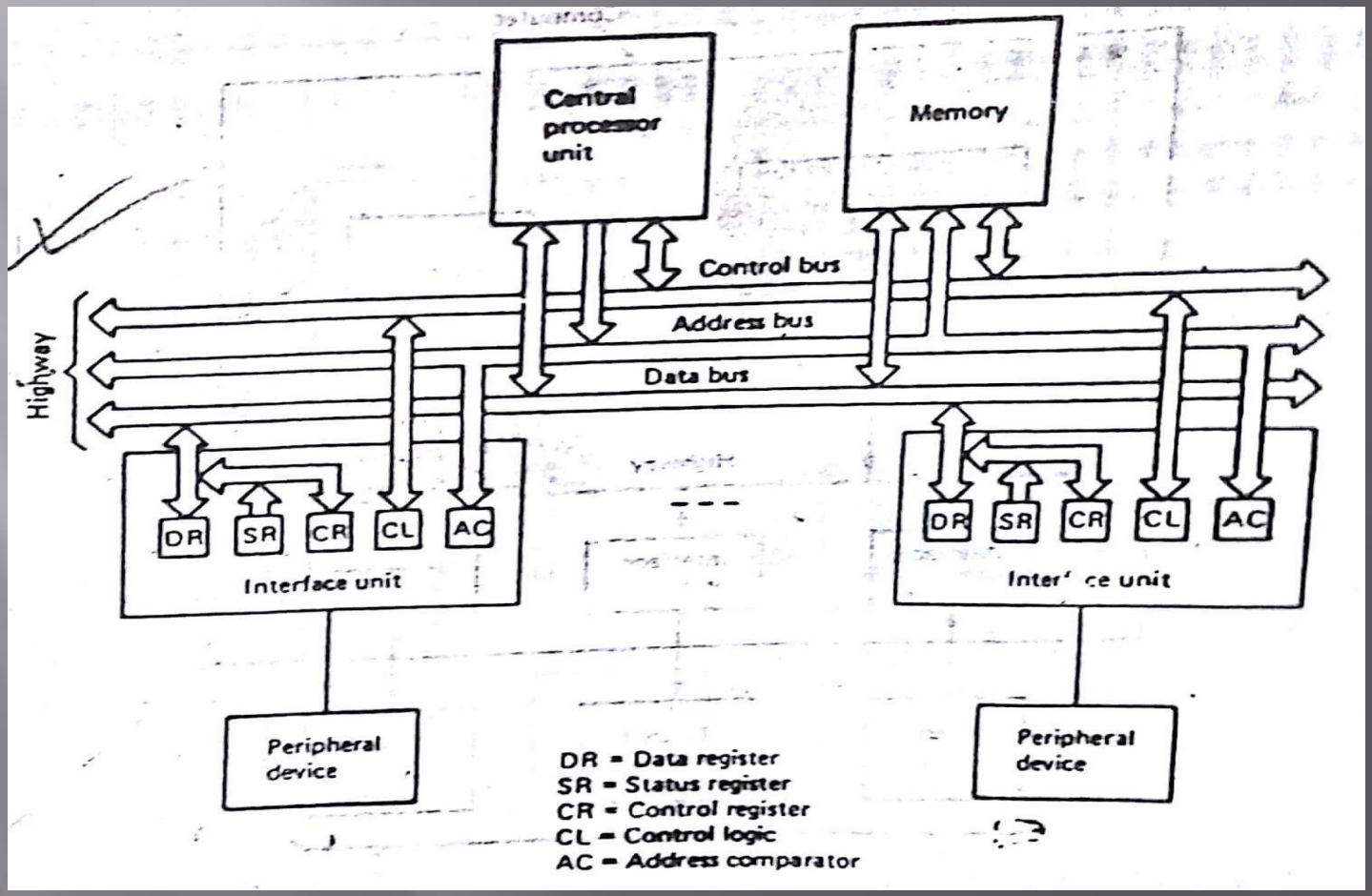
- ***Address Bus:***
  - It contains address information.
  - The number of lines available for this determines the maximum amount of physical memory that can be addressed.
  - If there are ***n*** lines , then 2^n locations can be addressed.
  - 8086 has 20 address lines and thus it can address 2^{20}=1048576 (1 Mega bytes) memory locations.

Computer Input-Output operations (Interface Unit)

- Interface unit is needed to ensure compatibility between the bus and the peripherals.
- Interface units are built into the computer and the points where the peripheral devices are connected are called I/O ports.

Computer Input-Output operations

(Interface Unit)



Typical Interface unit comprises

- Transmit data and receive data registers
- Control register
- Status register
- Address comparator
- Internal logic gates and circuitry

Input data to CPU

- Input data to the CPU from peripheral is done as follows:
  - Peripheral places its data in the received data register.
  - Sets the ready status flag
  - CPU is made to step periodically through all input peripheral addresses and test each ready status flag in turn
  - This way, discovers address of the ready peripheral: Software Polling
  - CPU uses this address and its I/Oinstructions to transfer data from the interface to the CPU. The program that do that is called device handlers or service routines.
  - Example instruction: IN A, (5)

Output data from CPU

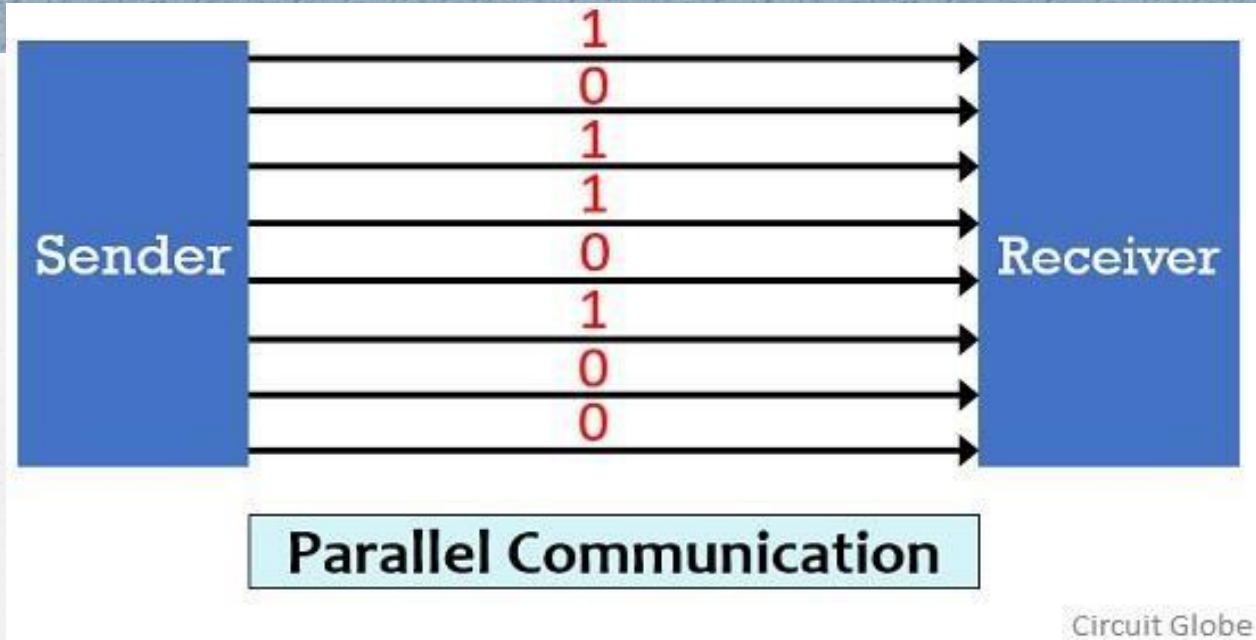
- CPU addresses the interface
- Test the status register
- If the relevant flag shows ready, CPU puts the data into interface unit transmit data register via the data bus
- Sets the control flag to show that there are some new data for the peripheral device.
- Example instruction: OUT (4), A

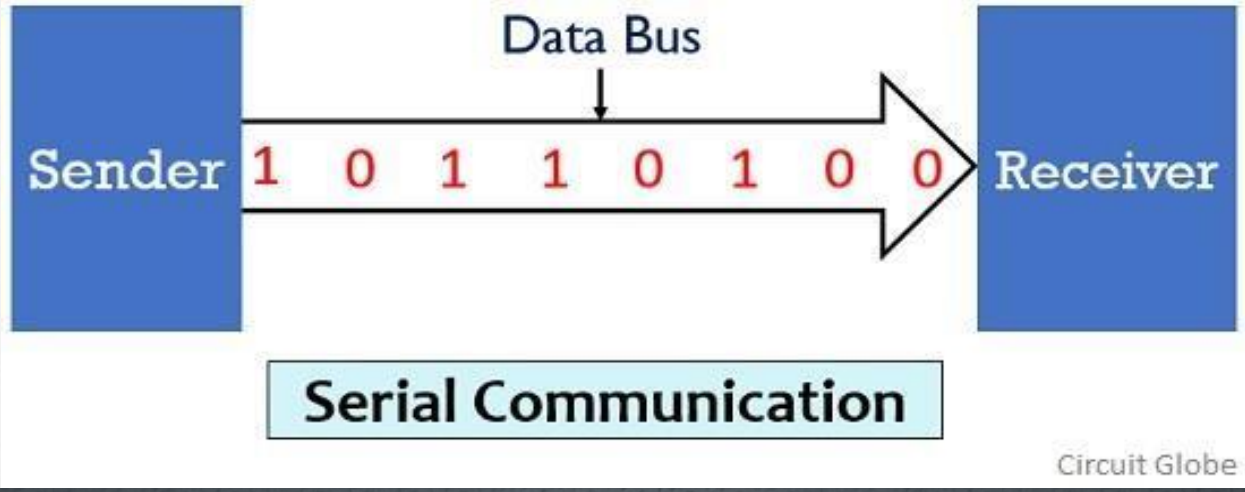
Week 2

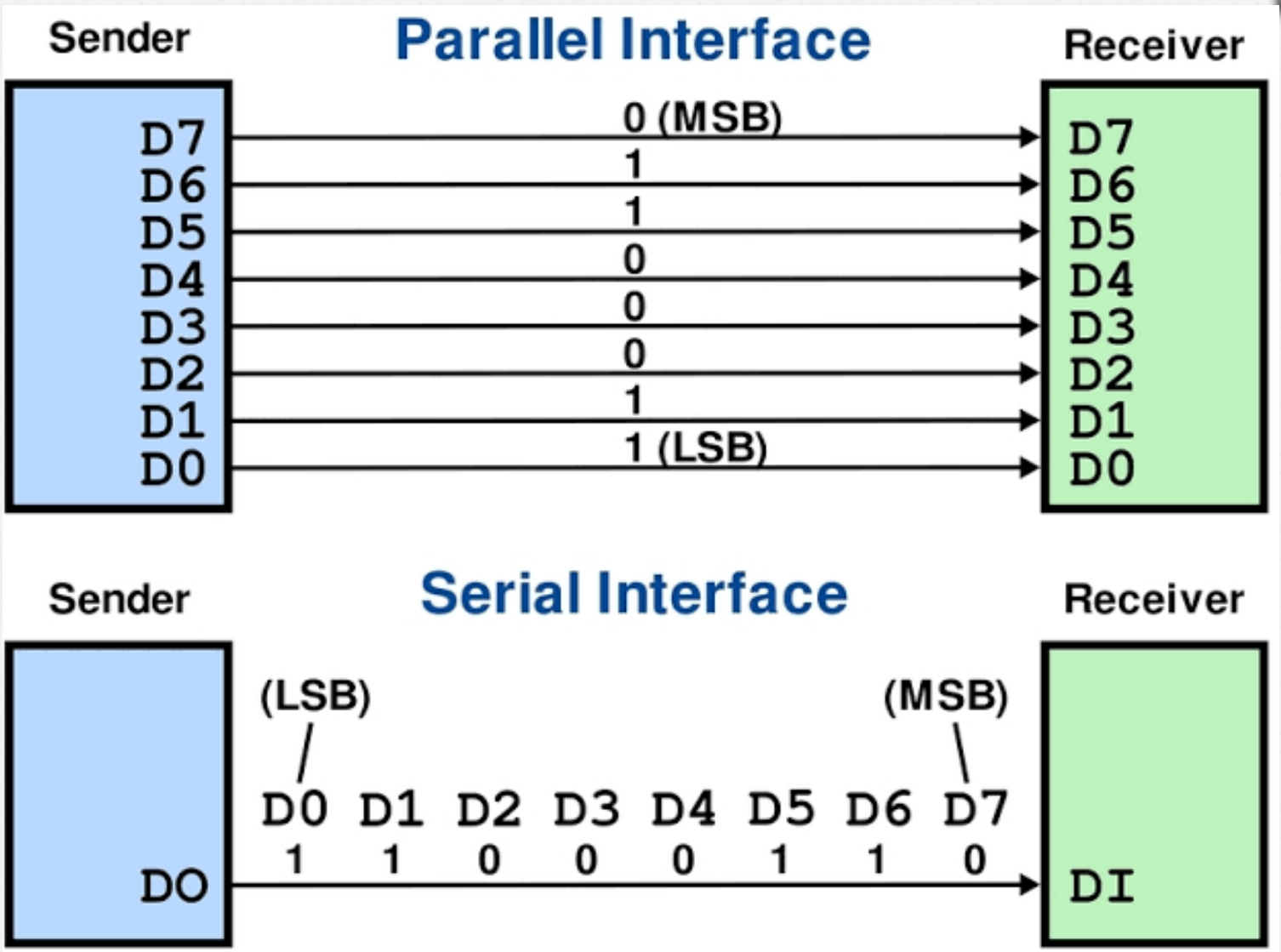
Serial And Parallel Transmission

There are two methods used to **transmit** data between digital devices: **serial transmission** and **parallel transmission**. **Serial** data **transmission** sends data bits one after another over a single wire. **Parallel** data **transmission** sends multiple data bits at the same time over multiple wires.

Normally Peripheral devices uses Serial data transmission. On the other hand, computer uses parallel data transmission concept.


Sender
1
0
1
1
0
1
0
0
Receiver
Parallel Communication
Circuit Globe


Sender
Data Bus
1 0 1 1 0 1 0 0
Receiver
Serial Communication
Circuit Globe


Sender
Parallel Interface
Receiver
D7
D6
D5
D4
D3
D2
D1
D0
0 (MSB)
1
1
0
0
0
1
1 (LSB)
D7
D6
D5
D4
D3
D2
D1
D0
Sender
Serial Interface
Receiver
(LSB)
(MSB)
D0 D1 D2 D3 D4 D5 D6 D7
1 1 0 0 0 1 1 0
DO
DI

Serial Interface

•Considered to be one of the most basic external connections to a computer, the **serial port** has been an integral part of most computers for more than 20 years. Although many of the newer systems have done away with the serial port completely in favor of USB connections, most modems still use the serial port, as do some printers, PDAs(Personal Device Assistant) and digital cameras.

•Essentially, serial ports provide a standard connector and protocol to let you attach devices, such as modems, to your computer.

Serial Interface

The name "serial" comes from the fact that a serial port "serializes" data. That is,
it takes a byte of data and transmits the 8 bits in the byte one at a time.

The advantage is that a serial port needs only one wire to transmit the 8 bits (while a parallel port needs 8). So to send data in long distance it may be converted in serial form. Serial ports lower cable costs and make cables smaller.

The disadvantage is that it takes 8 times longer to transmit the data than it would
if there were 8 wires.

Serial Interface

Serial ports, also called **communication (COM) ports**, are **bi-directional**.

Bi-directional communication allows each device to receive data as well as transmit it. Serial devices use different pins to receive and transmit data -- using the same pins would limit communication to **half-duplex**, meaning that information could only travel in one direction at a time.

Using different pins allows for **full-duplex** communication, in which information can travel in both directions at once.

Serial Interface

- **Data is moved in parallel within a computer. To interface a computer with serial data lines, the data must be converted to and from serial form.**
- **A parallel-in-serial-out shift register and a serial-in-parallel-out shift register can be used to do this.**

Parallel-Serial Conversion

- **For Transmission, parallel data word is loaded into the shift register.**
- **A pulse on the clock input causes the data to be shifted.**
- **For an n-bit data word n clock pulses will output the word in serial form.**

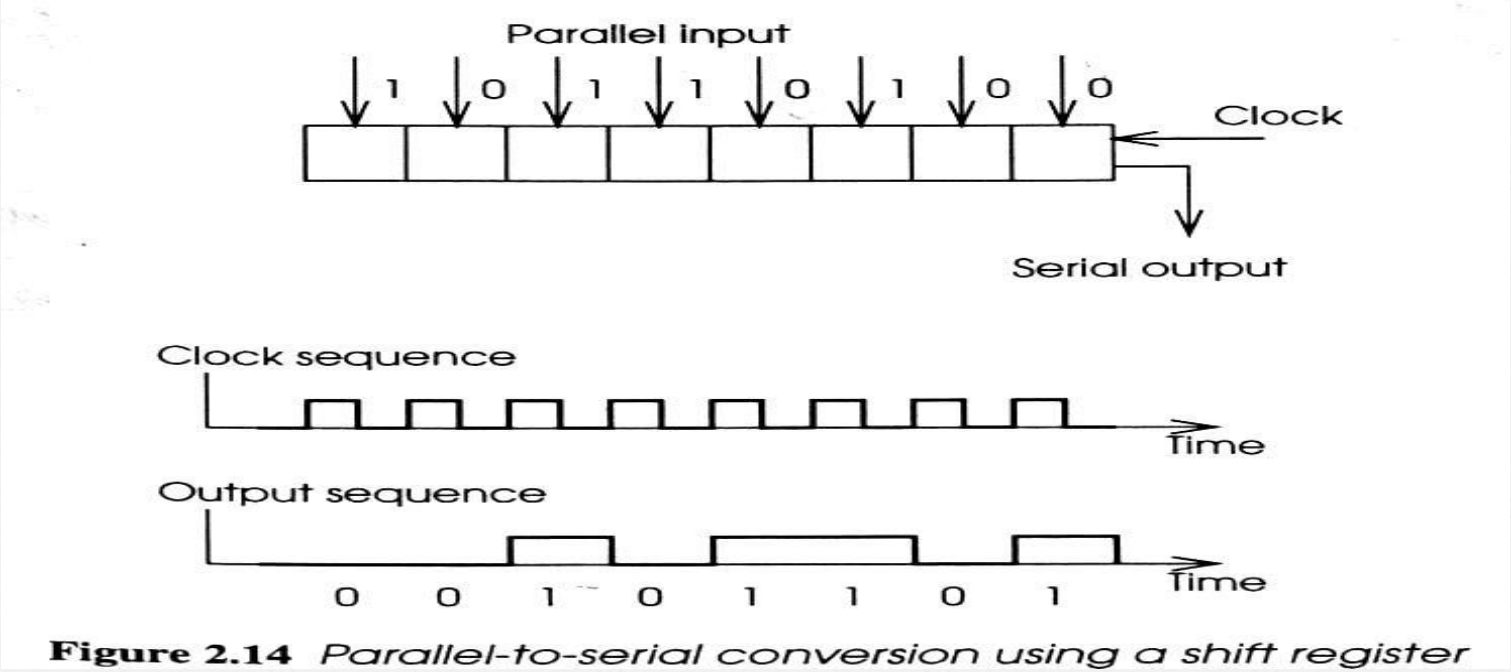


Figure 2.14 *Parallel-to-serial conversion using a shift register*

Serial-Parallel Conversion

- **Reception of the serial data is performed by another shift register, in a serial-to-parallel convertor.**
- **Asequence of n clock pulses causes the input to propagate along the shift register until it is all available in parallel.**
- **The first bit to arrive is shifted all the way through the shift register and appears at the right hand end.**

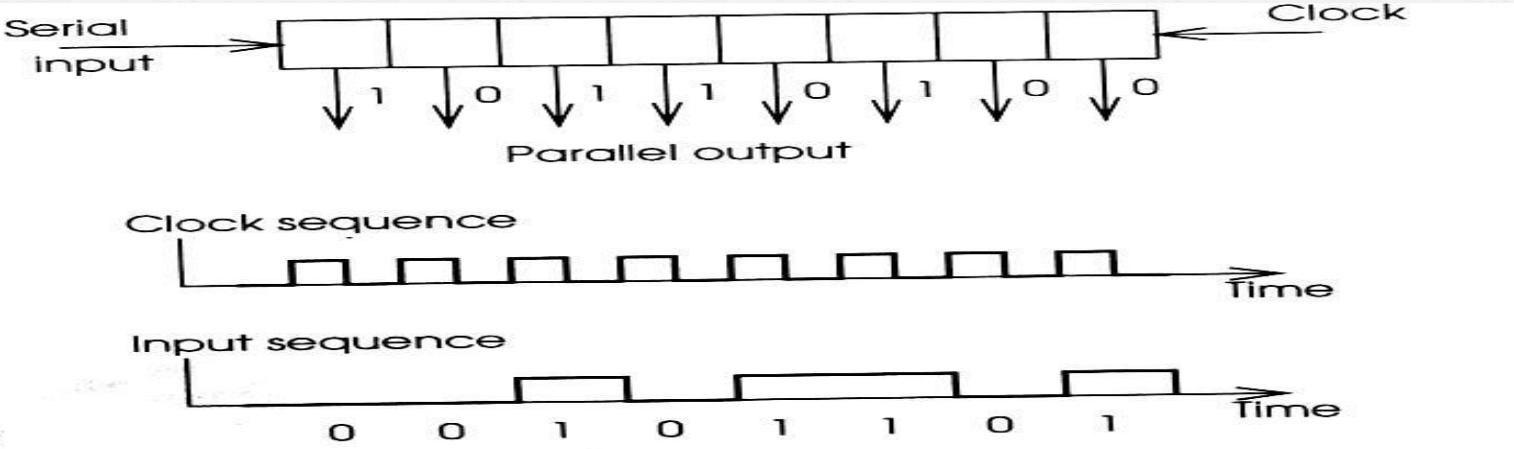
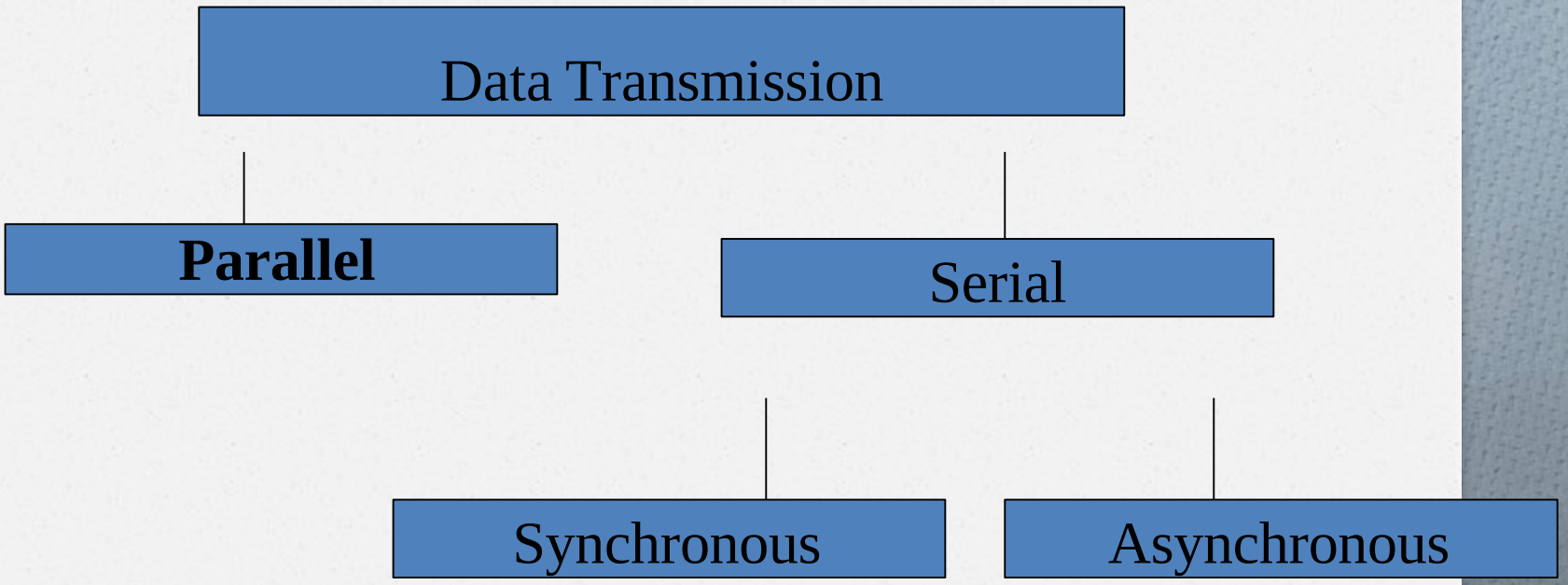


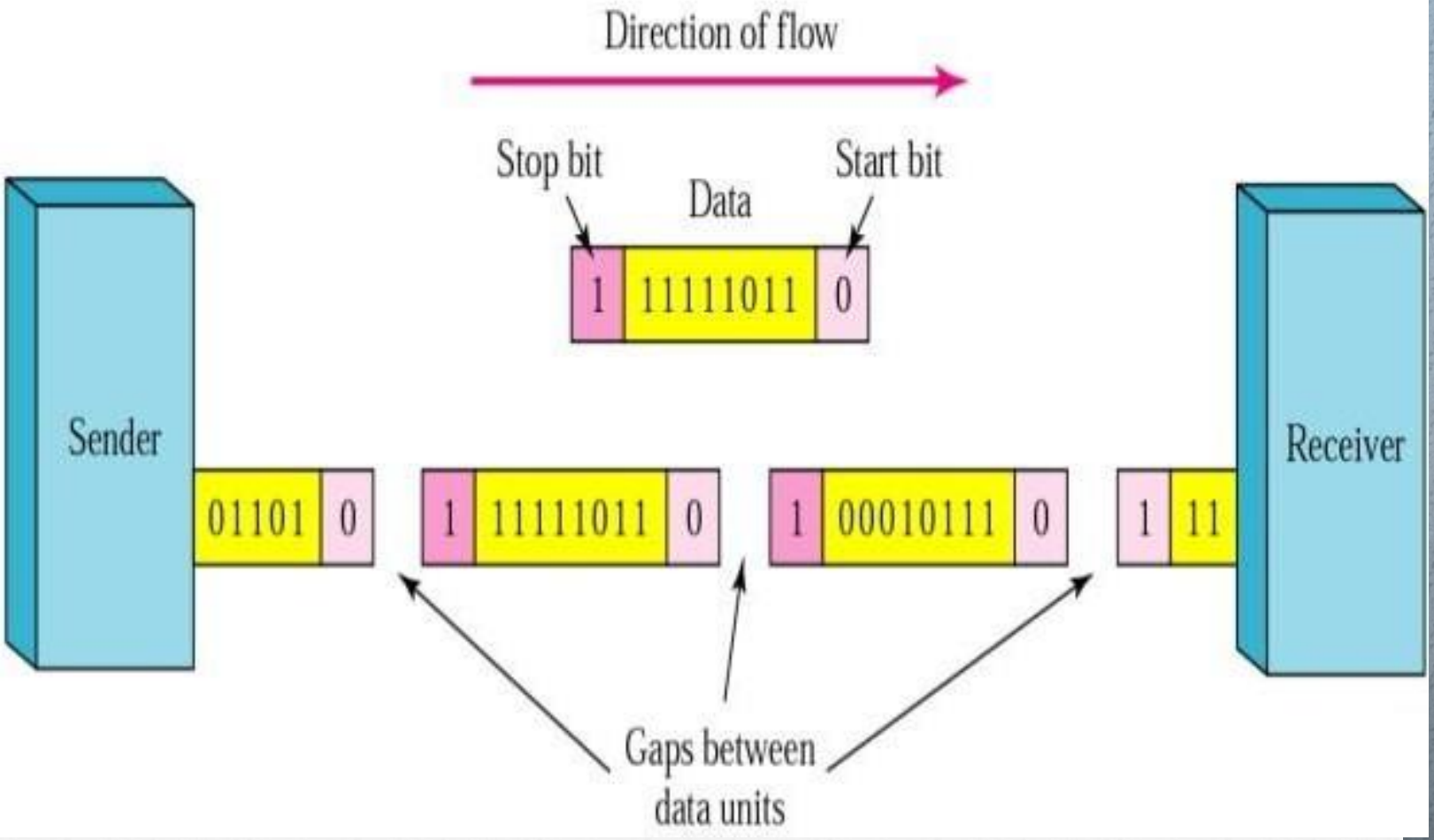
Figure 2.15 *Serial-to-parallel conversion using a shift register*

Data Transmission Tree



Week 3

Asynchronous Transmission



Asynchronous Transmission

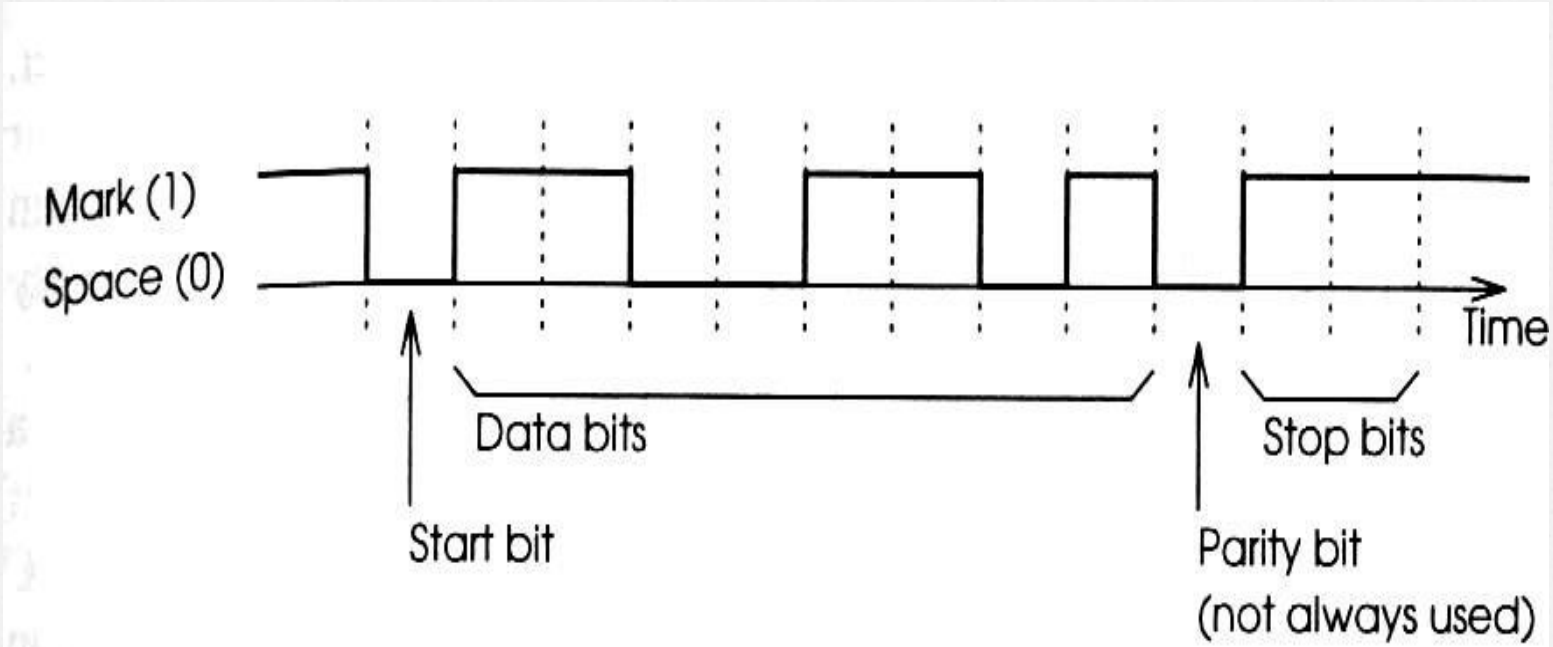


Figure 2.16 *Asynchronous character format*

Definitions

Start

- **Bit**
  - Signals the beginning of the data word
  - A low bit after a series of high bits
- **Data Bits**
  - The meat of the transmission
  - Usually 7 or 8 bits

Definitions Continued

Parity Bit

- An error check bit placed after the data bits
- Can be high or low depending on whether odd parity or even parity is specified

Stop Bit/s

- One or two high bits that signal the end or the data word

Data Word

- Start Bit, Data Bits, Parity Bit, & Stop Bit/s

In **Synchronous transmission** data is sent in the form block by block. This transmission is the full duplex type. Between sender and receiver the synchronization is compulsory. In Synchronous transmission, There is no gap present between data. It is more efficient and more reliable than asynchronous transmission to transfer the large amount of data.

On other hand in **Asynchronous transmission** data is **transmitted** in the form of byte or character. This transmission is the half duplex type transmission. In this transmission start bits and stop bits are added with data. It does not require synchronization.

SL. No	Synchronous Transmission	Asynchronous Transmission
01	In Synchronous transmission, Data is sent in form of blocks or frames.	In asynchronous transmission, Data is sent in form of byte or character.
02	Synchronous transmission is fast.	Asynchronous transmission is slow.
03	Synchronous transmission is costly.	Asynchronous transmission less costly.
04	In Synchronous transmission, There is no gap present between data.	In asynchronous transmission, There is present gap between data.
05	Efficient use of transmission line is done in synchronous transmission.	While in asynchronous transmission, transmission line remains empty during gap in character transmission.
06	Synchronous transmission needs precisely synchronized clocks for the information of new bytes.	Asynchronous transmission have no need of synchronized clocks as parity bit is used in this transmission for information of new bytes.
07	It is full duplex mode communication	It is half duplex mode communication.

Bit Rate and Baud Rate

- **Bit rate** is a measure of the number of data bits (that's 0's and 1's) transmitted in one second.

- **Baud Rate(signal unit/ sec)**
  - The number of signal units per second
  - Less than or equal to the bit rate

Synchronous Transmission

- Data are sent continuously.
- There is no start bit to indicate where a character begins. So this must be achieved by special sequence of data known as protocol.
- One such protocol HDLC – High Level Data Link Control format is shown below:

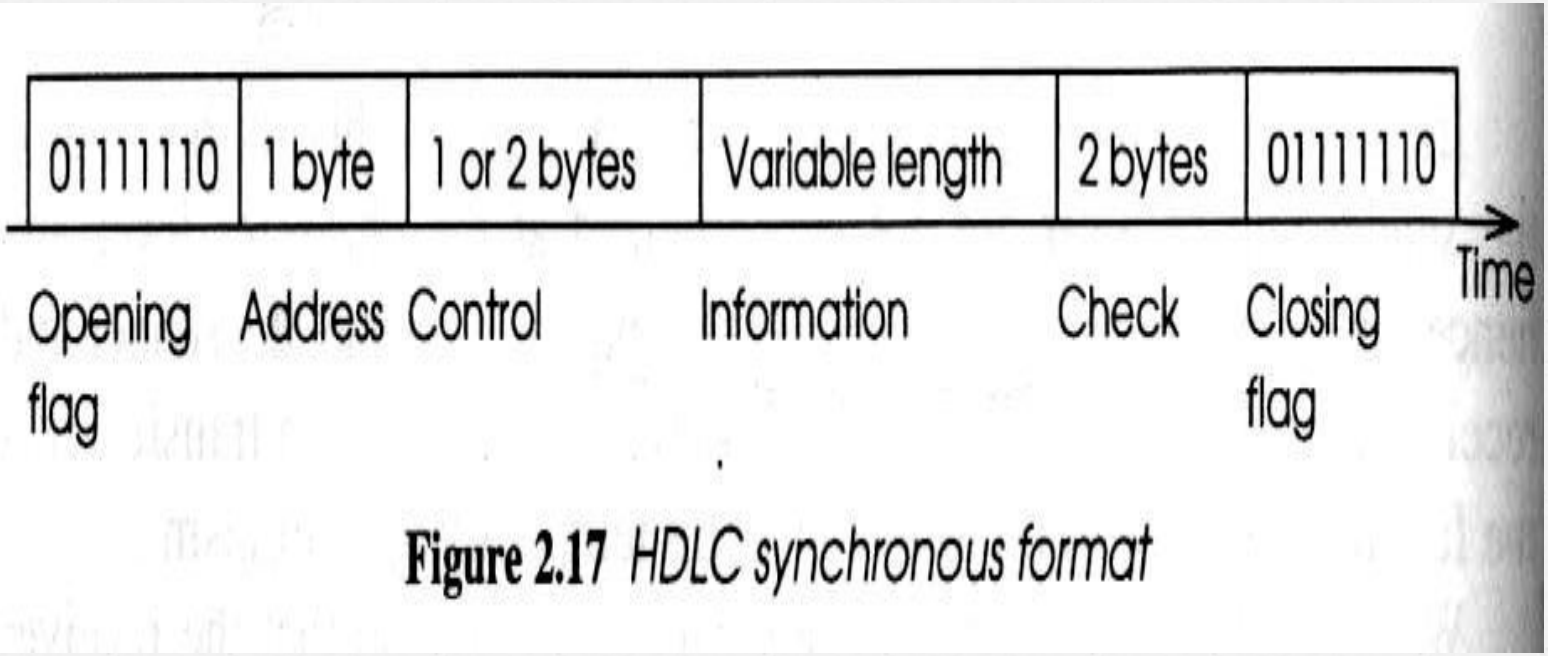


Figure 2.17 *HDLC synchronous format*

Synchronous Transmission: Bit Stuffing

- Character synchronization is achieved by identifying a special pattern of bits (01111110) known as a Flag.
- This pattern is unique and can never occur in the data stream except as a flag.
- Since the flag contains 6 consecutive 1s, data to be transmitted is checked for 5 consecutive 1s and if found a 0 is inserted after them. This technique is called *Bit Stuffing*.
- At receiving end, to removing these additional stuff bit and getting back the original data frame is called bit un-stuffing

Bit Stuffing

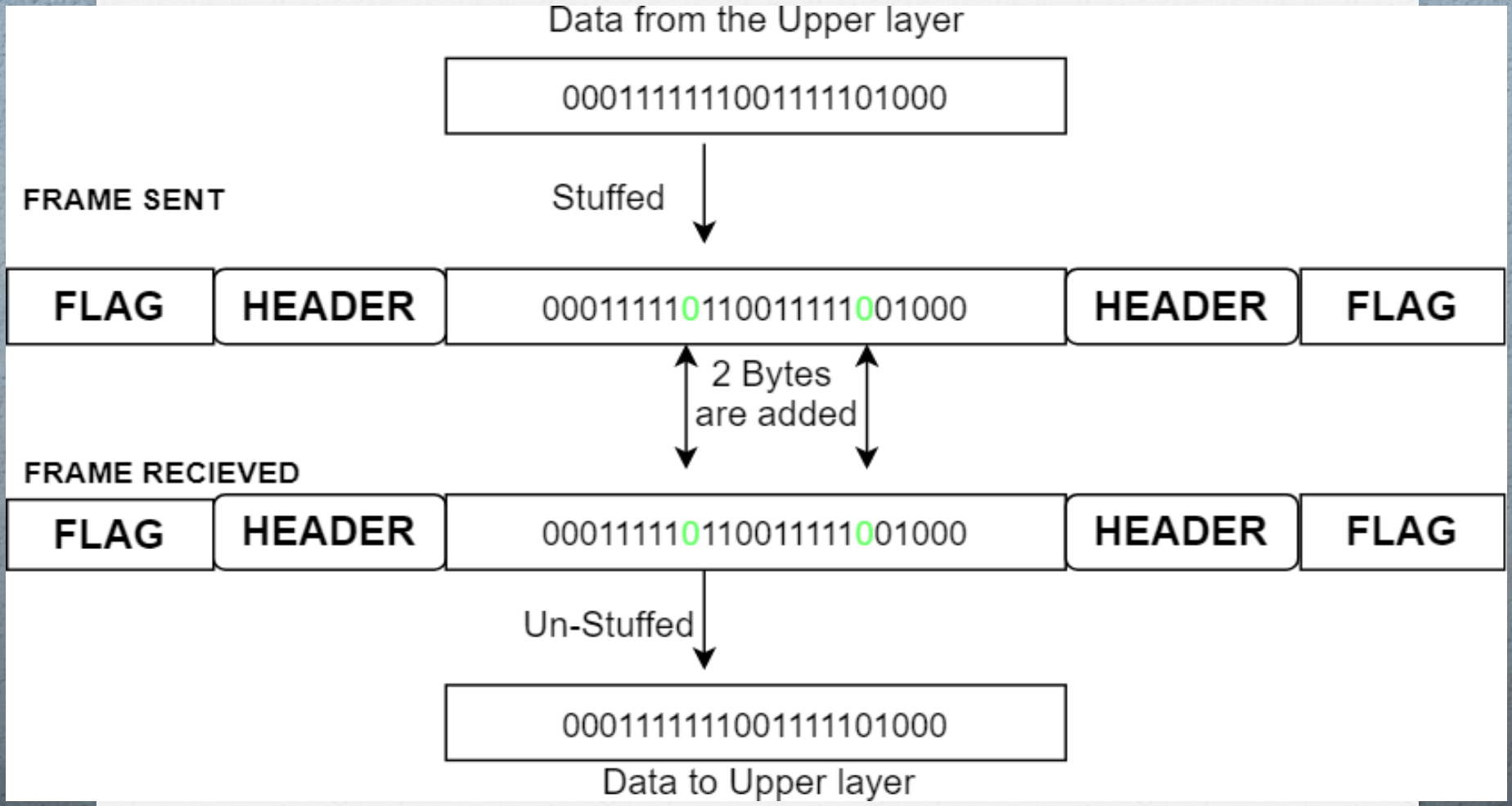
Definition: Bit Stuffing is the process of inserting non-information bits into data to break up bit patterns to affect the synchronous transmission of information. It is widely used in network and communication protocols, in which bit stuffing is a required part of the transmission process.

Each frame begins and ends with a special bit pattern called flag byte [01111110].

Whenever sender data link layer encounters five consecutive ones in the data stream, it automatically stuffs a 0 bit into the outgoing stream.

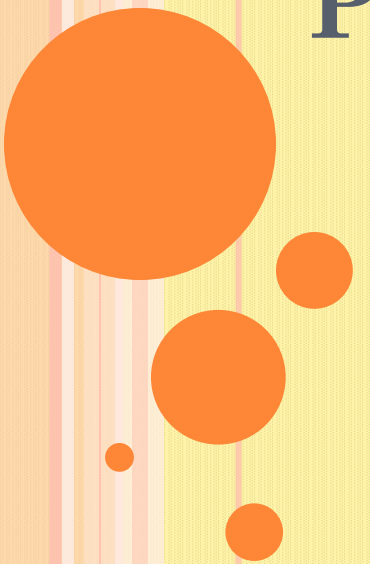
When the receiver sees five consecutive incoming ones, it automatically unstuffs the 0 bit before sending the data to the network layer.

Bit Stuffing and Bit Un-stuffing



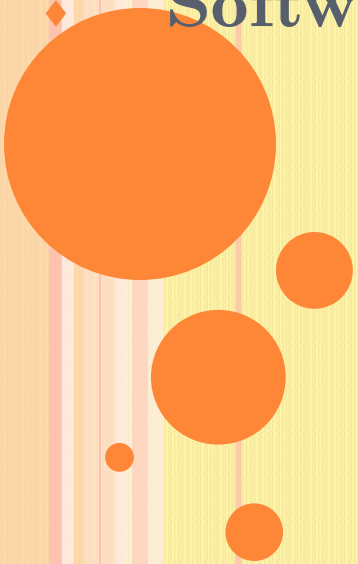
Week 4

INTERRUPTS IN PERIPHERALS



Types of Interrupts

- External interrupts
- Internal interrupts
- Software interrupts



External Interrupts

- ***External interrupts*: are used by the CPU to interact with nput/output devices.**

External interrupts improve system performance by allowing the CPU to execute instructions, instead of just waiting for the I/O device, while still performing the required data transfers.

Internal Interrupts

- ***Internal interrupts*: occur entirely within the CPU; no input/output devices play any role in these interrupts.**

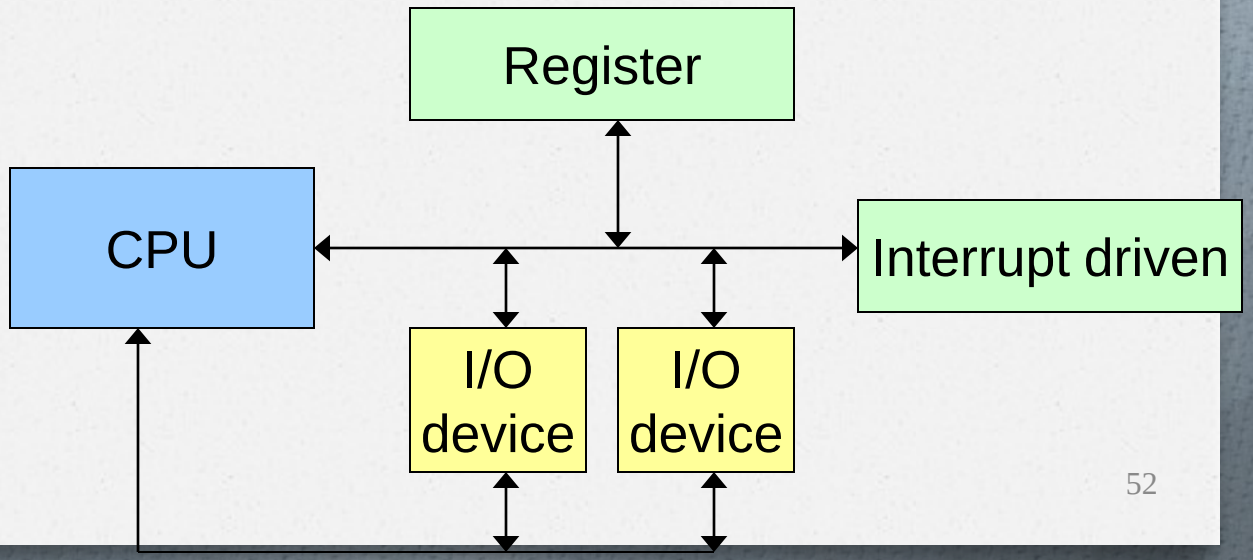
Internal interrupts could be used to allocate CPU time to different tasks in a multitasking operating system. This interrupts can also be used to handle exceptions that occur during the execution of valid instructions.

How Interrupts Are Handled?

- Different routines handle different interrupts – called Interrupt Service Routines (ISR).
- When CPU is interrupted
  - It stops what it was doing, and context is saved.
  - A generic routine called **Interrupt Handling Routine** (IHR) is run which
    - Examines the nature of interrupt
    - Calls the corresponding **Interrupt Service Routine** (ISR) -- stored in lower part of memory.
- After servicing the interrupt, the saved address is loaded again to PC to resume the process again.

General Interrupt Flow

1. Completes current instruction
2. Saves current state to status registers
3. Identify source
4. Jump to and activate Interrupt Service Routing (ISR)
5. Return to original program (RTI) and restore state



How Interrupts Are Handled?

(Continued)

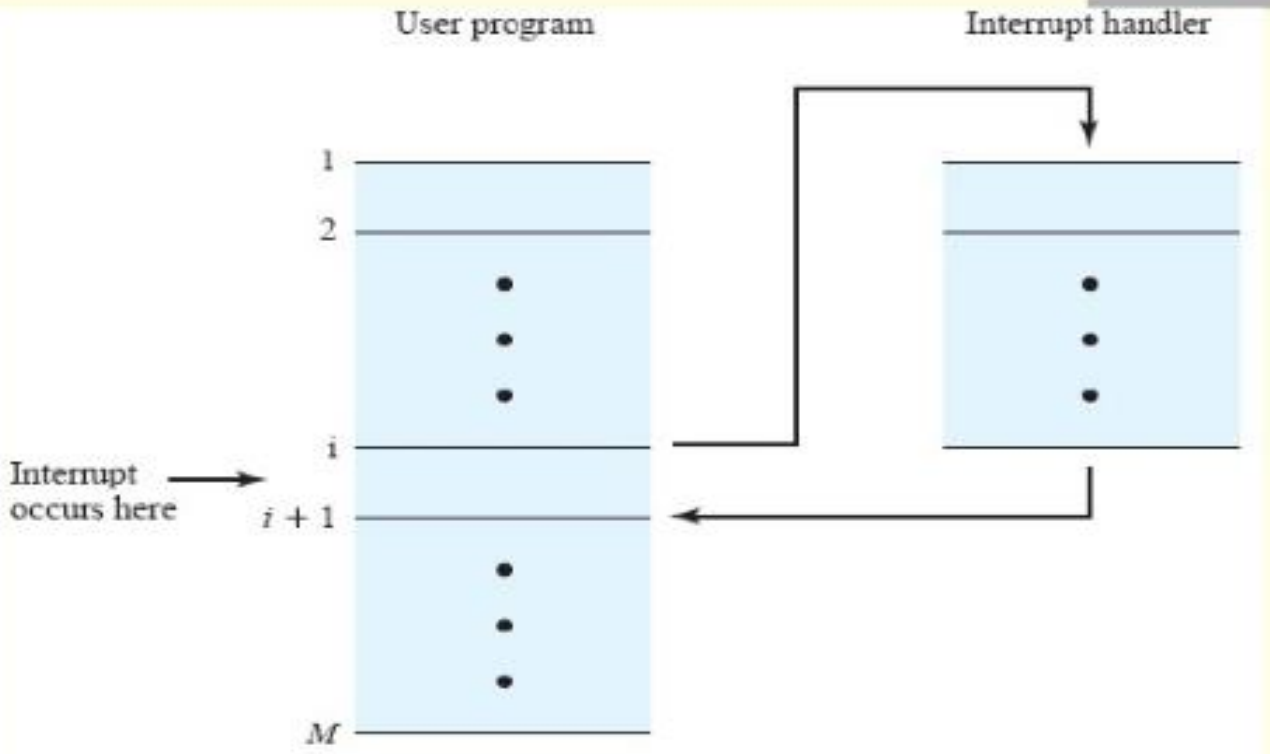
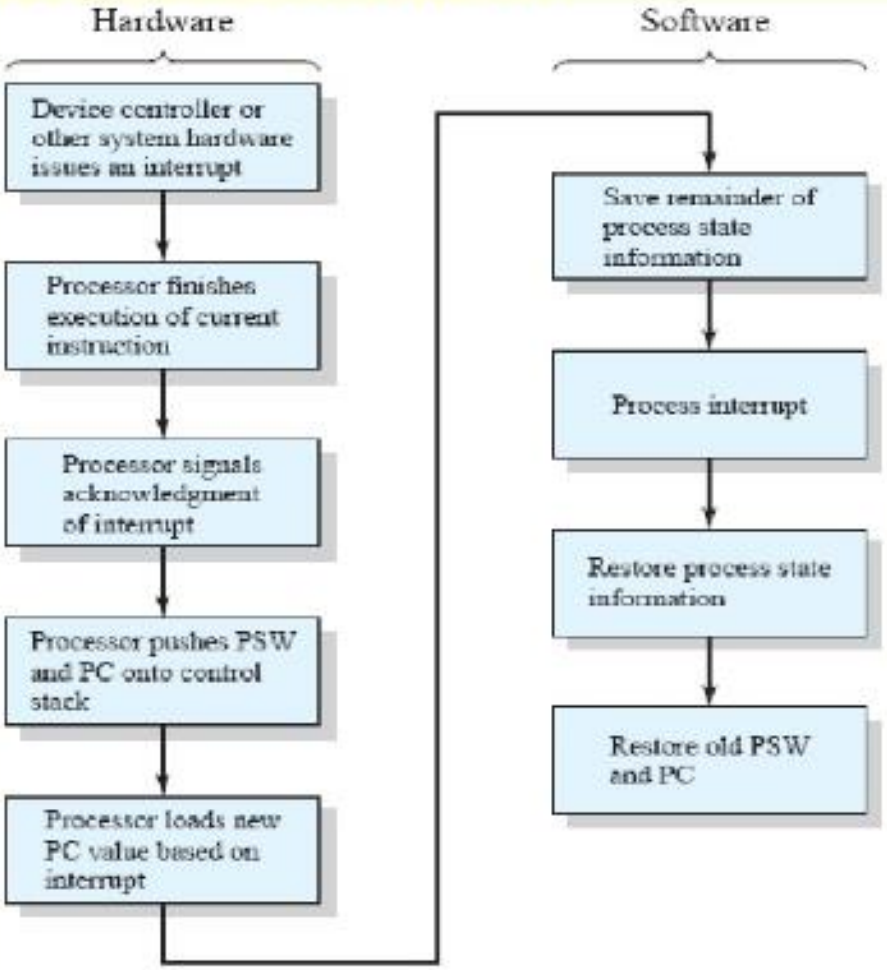


Figure Transfer of Control via Interrupts

How Interrupts Are Handled?

(Continued)

- Interrupt Processing



Types of interrupts

- Ignorable interrupts (or Maskable)
  - Most often used
  - Good for using when computer needs to do something more important
  - When the interrupt mask is set, interrupts are hidden and therefore are ignored.
- Non-ignorable interrupts (Non-maskable)
  - NMI's take precedence and interrupt any task

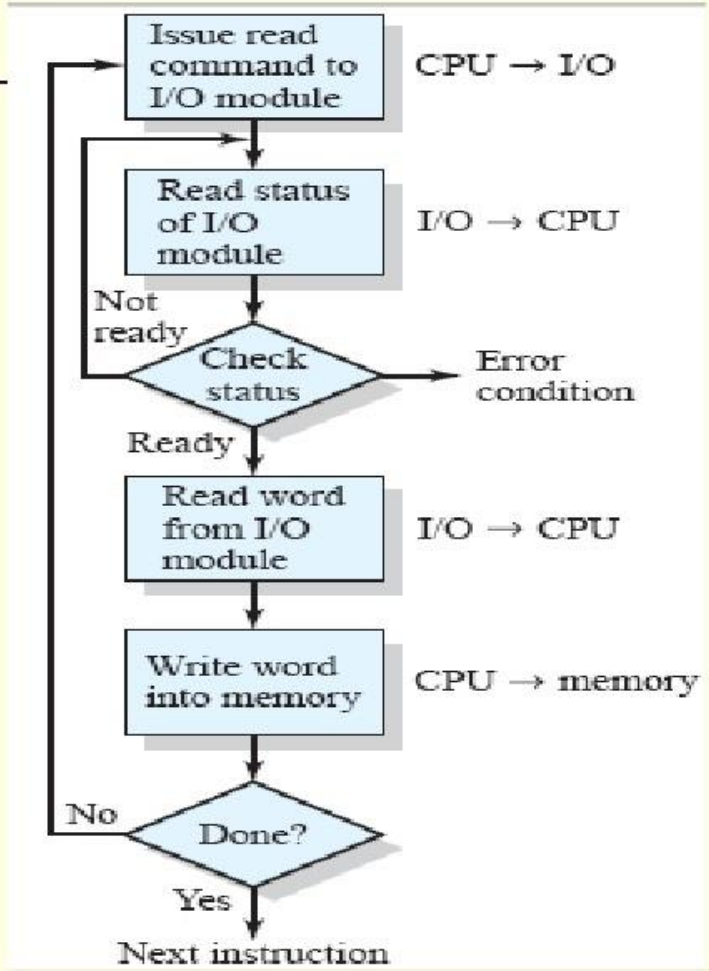
Input Output method and Computer (Memory) Communication procedure

I/O COMMUNICATION TECHNIQUES

- Three techniques are possible for I/O operations
  - Programmed I/O
  - Interrupt-driven I/O
  - Direct memory access (DMA)

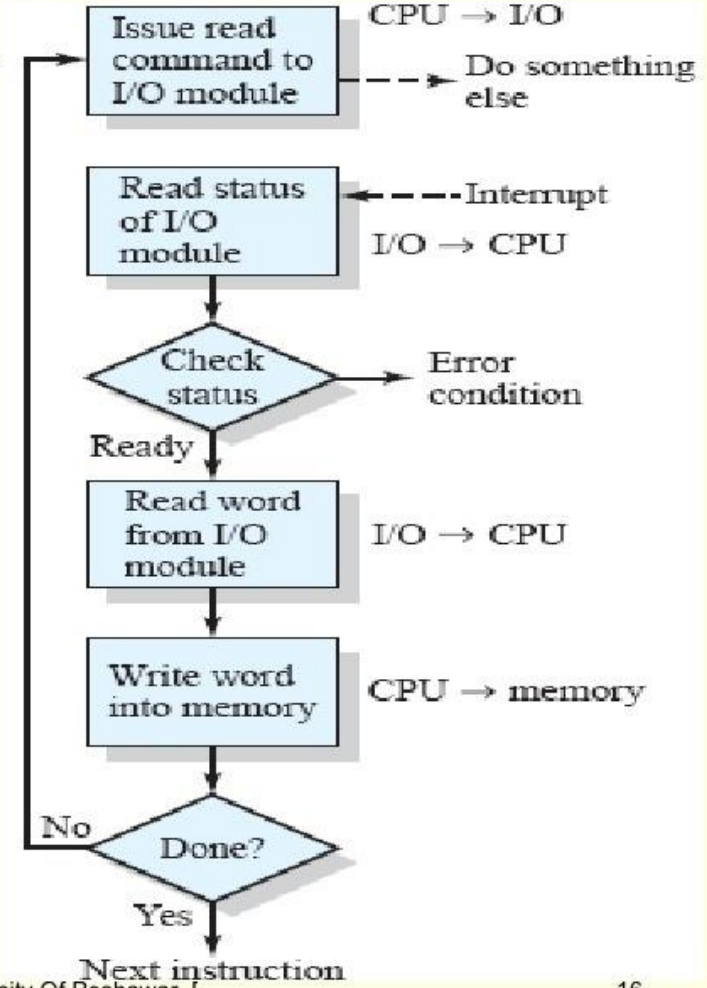
Programmed I/O

- CPU while executing a program encounters an I/O instruction
- CPU issues I/O command to I/O module
- I/O module performs the requested action & set status registers
- CPU is responsible to check status registers periodically to see if I/O operation is complete. **SO**
- No Interrupt to alert the processor



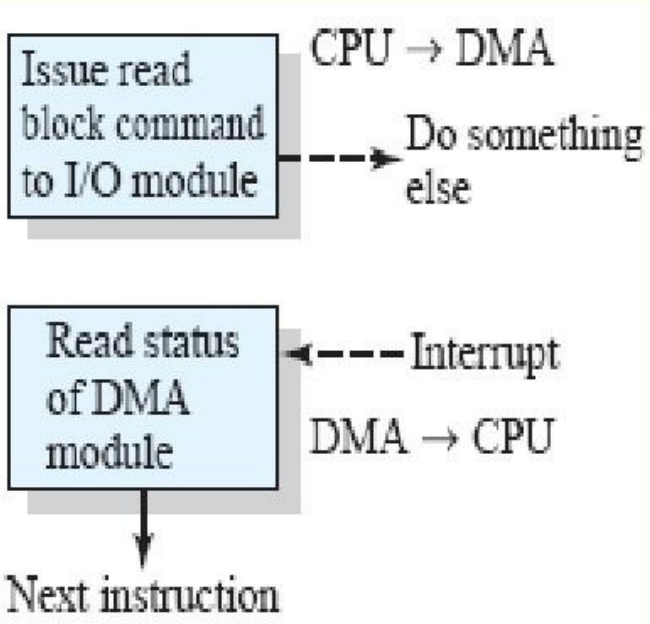
Interrupt-Driven I/O

- Similar to direct I/O but processor not required to poll device.
- I/O module will interrupt CPU for data exchange when ready



Direct Memory Access (DMA)

- I/O exchanges occur directly with memory
  - Requires DMA module on system bus
  - Capable of mimicking CPU and taking over control of system from CPU
  - DMA will use bus when
    - Processor does not require it OR
    - Must force processor to suspend operation temporarily– called cycle stealing
- An interrupt is sent when the task is complete
- The processor is only involved at the beginning and end of the transfer



Week 5

How to Access the Interrupt Handler?

1. CPU pushes the return address on to the stack

2. Reads in the interrupt vector

3. Jumps to the address corresponding to this vector, 1111(vector) 0000.

8086 with 8259A

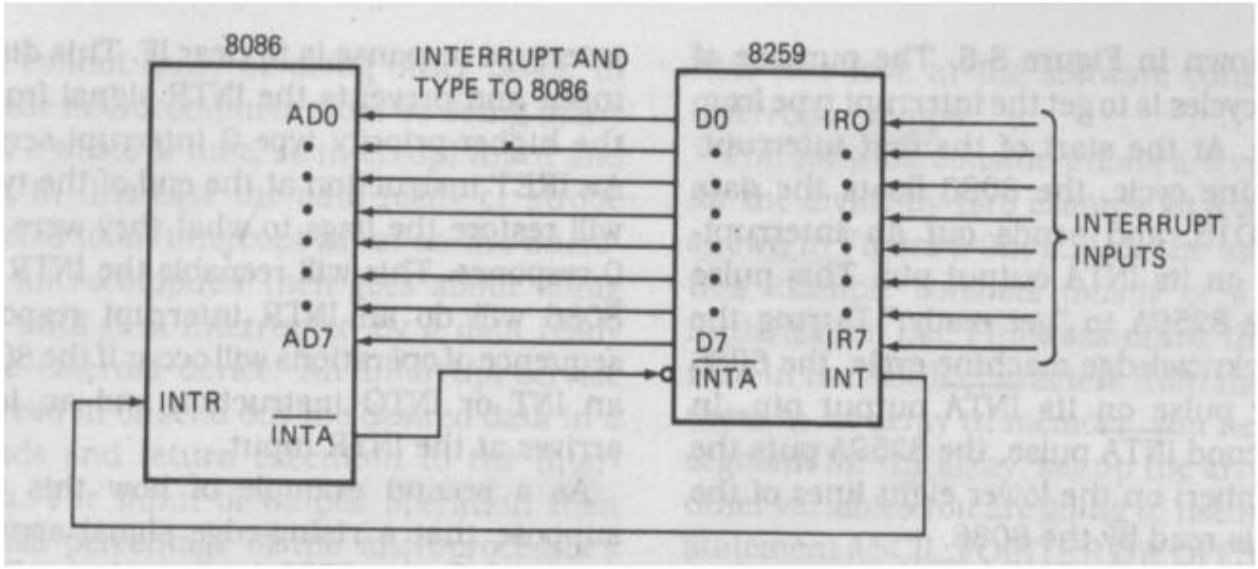


Figure: Block diagram showing an 8259 connected to 8086

Why 8259A

8086 effectively have only two input pins for interrupt input. NMI and INTR.

The NMI interrupt input pin is normally assigned for a power failure interrupt.

It leaves 8086 with only one interrupt input pin.

8259A is used to funnel interrupt requests from multiple sources to a single INTR pin of the 8086.

Block diagram of 8259A

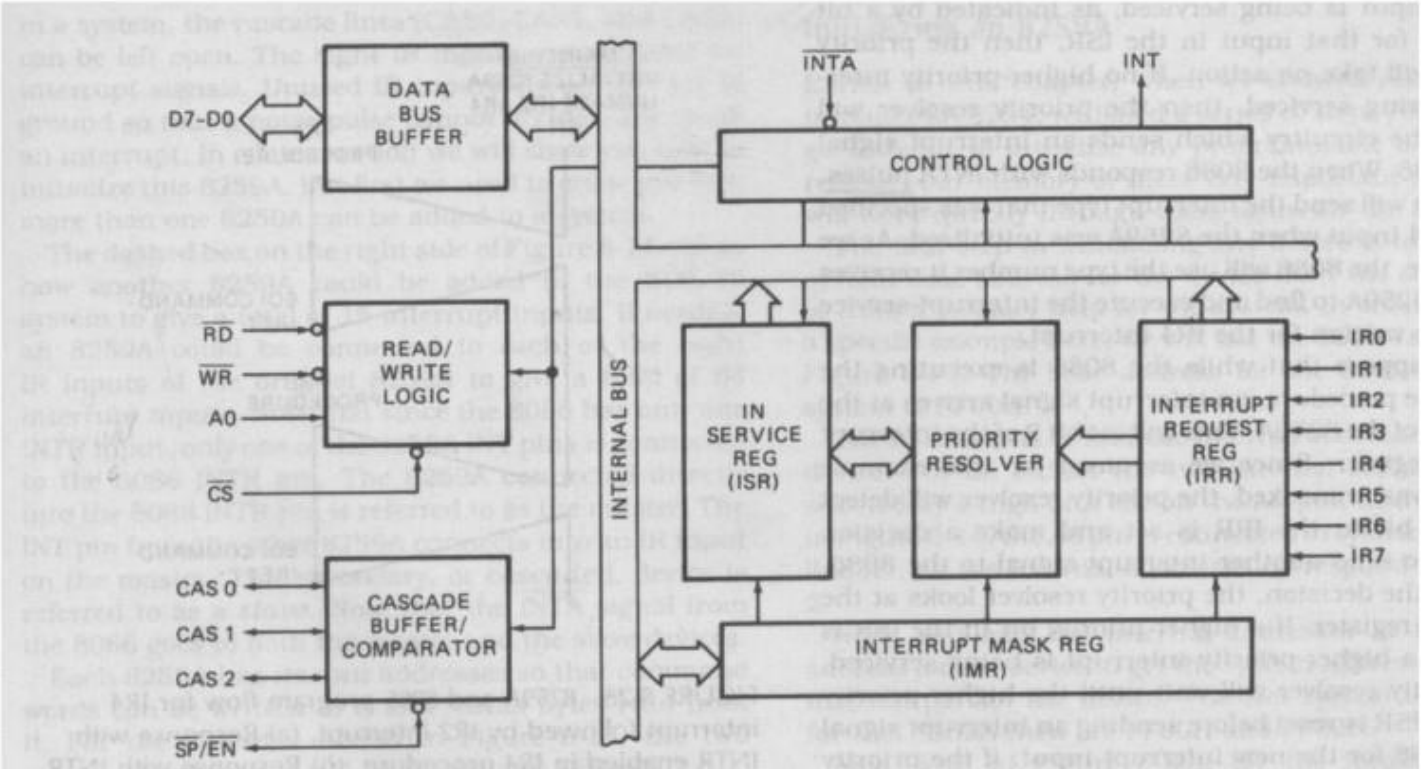


FIGURE 8-27 8259A internal block diagram. (*Intel Corporation*)

1. Data Bus Buffer

Receive interrupt type and sends it to 8086

Send control words to the 8259A

Read a status word from 8259A

These transfers are controlled by RD and WR pin when this device is selected by CS pin.

2. Control Logic

The INTA input of 8259A is connected to INTA output of 8086

The INT output of 8259 is connected to the INTR input of the 8086

There are eight interrupt request inputs (IR0 - IR7) on the right side of the diagram.

If 8259A is properly enabled, an interrupt signal applied to any of these inputs will cause the 8259A to assert its INT output pin HIGH. If this pin is connected to the INTR pin of 8086 and 8086 interrupt flag is set, then 8086 will do the following responses:

3. Registers

Interrupt Request Register

Keeps track of which interrupts are asking for service. If a signal comes in the IR inputs the corresponding bit in the IRR register will be set.

Interrupt Mask Register

Used to enable (Unmask) or disable (Mask) specific interrupts.
Each bit in this register corresponds to the interrupt input with same number.
To unmask a particular interrupt send a command word with a zero in the corresponding bit.

In Service Register

Keeps track of which interrupts are currently in service. Used for priority interrupt handling. The corresponding bit of the current interrupt in service is SET.

Connections

- The CAS0, CAS1 and CAS2 are used to cascade 8259A chips to get more than 8 interrupts. If only one chip is used they are left open
- Unused IRs must be tied to the ground.
- SP/EN is tied to high if only one 8259A is used.

Week 6

DMA

Features Of DMA

>> The activity involved in transferring a byte or word over the system bus is called a bus cycle.

>> During bus cycle one component must be the master – which will have complete control over the bus. Taking control of the bus for a bus cycle is called cycle stealing.

>> DMA is a data transfer technique between Main Memory and External device. It can be used to memory to memory transfers also.

>> There is no involvement of Microprocessor.

>> DMA controller controls the Main Memory in the same way the Microprocessor do.

>> Ensures very high data transfer rate. Because the data transfer is handled totally in hardware.

>> Microprocessor and DMA controller gets control of data, address and control bus by time sharing.

Steps to Perform DMA

1) Interface of the external Device (DMA requesting I/O device) activates the DREQ line high to send a request for DMA service to the controller.
2) The DMA controller sends a bus request to the microprocessor through its HOLD pin.
3) After the current bus cycle is complete the microprocessor will respond by putting a 1 on the HLDA (HOLD Acknowledge)pin to DMA controller. When the requesting device receives this grant signal it becomes the master. It will remain master until it drops signal to the HOLD pin, at which time 8086 will drop the grant on the HLDA pin.

4) After receiving HLDA, DMA controller sends out a signal and takes the full control of Data, Address and Control buses.

5) DMA controller puts the content of the address register on the address bus..

6) DMA controller sends a DACK signal to the interface to tell it to put
data on data bus.

7) At the same time DMA controller asserts appropriate signals to IOR/IOW and MEMW/MEMR pins.

8) Bytes of data are transferred to the memory location indicated by the address bus .

9) After completion of DMA, DMA controller releases
   a) its hold request HOLD to the processor.
   b) control of buses.

10) The address register is incremented by 1.

11) The byte count register is decremented by 1.

12) If the byte count register is non-zero, return to step 1;otherwise stop.

DMA CONTROLLER

- A DMA controller is capable of becoming the bus master and supervising a transfer between an I/O interface and memory.
- A DMA controller is designed to service one or more I/O interfaces and each interface is connected to the controller by a set of conductors.
- A portion of a DMA controller for servicing a single interface is called a **channel.**
- It has n channels for n different I/O devices. 8237 has 4 channels.

A DMA controller has control and status register.There is also a temporary register.

And Each channel contains

>>Address Registers (base and current)

>>Byte count register(base and count)

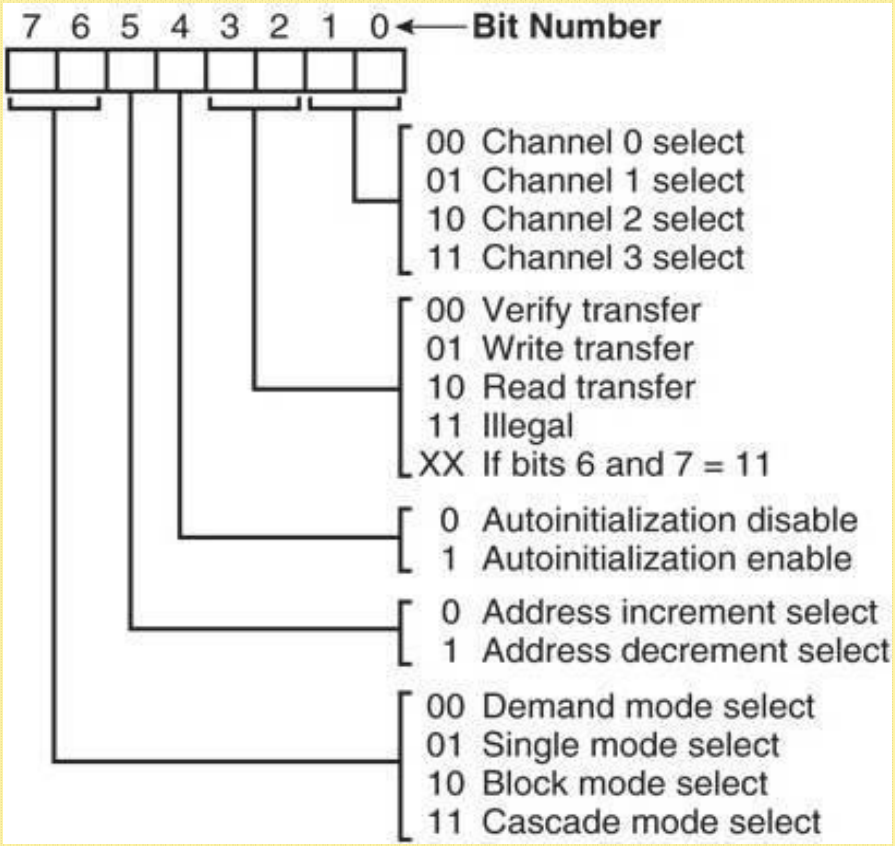
>> Mode register

>>Request flag and Mask flag

Week 7

Mode Register

- The mode register programs the mode of operation for a channel.
- Each channel has its own mode register as selected by bit positions 1 and 0.
  1. Remaining bits of the mode register select operation, auto-initialization, increment/decrement, and mode for the channel

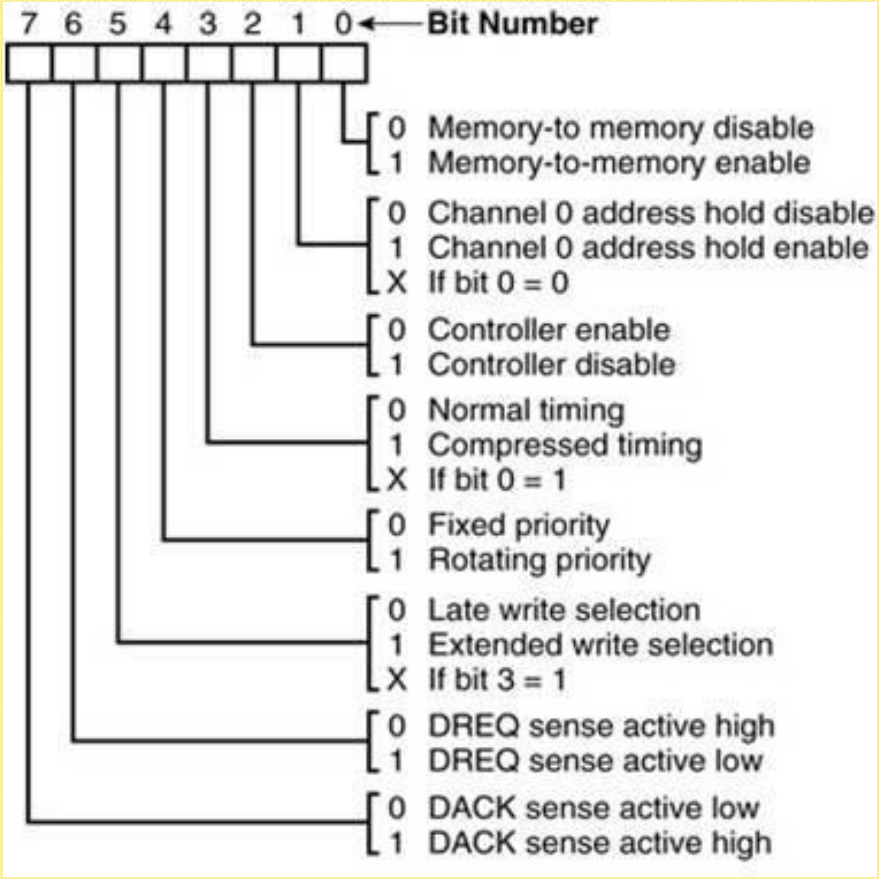


Control/Command Register

The command register programs the operation of the 8237 DMA controller.

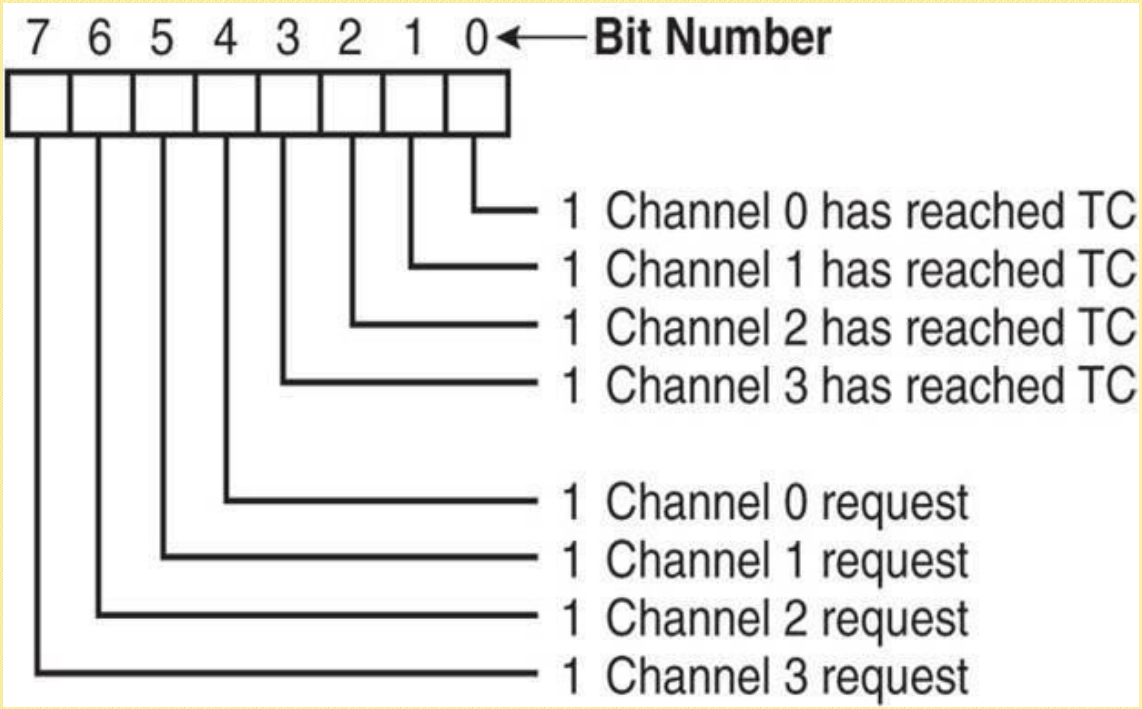
The register uses bit position 0 to select the memory-to-memory DMA transfer mode.

- Memory-to-memory DMA transfers use DMA channel
- DMA channel 0 to hold the source address
- DMA channel 1 holds the destination address



Status Register

The status register shows status of each DMA channel. The TC(Terminal Count) bits indicate if the channel has reached its terminal count (transferred all its bytes).
When the terminal count is reached, the DMA transfer is terminated for most modes of operation.
The request bits indicate whether the DREQ input for a given channel is active. The 8237 is activated by DREQ to continue the transfer until a TC is reached



Week 8

Block Data Transfer

- To transfer blocks of data between memory and peripheral devices, following information are needed.
  - Peripheral device address
  - Starting address of the block allocated in the memory
  - Number of data words in the block
  - Direction of transfer

CPU CONTROLLED BLOCK DATA TRANSFER

- CPU uses special block data transfer instructions
- CPU monitors the whole operation
- Disadvantage is CPU is not free to do other tasks

Codes

- Different types of characters:
  - Numeric (0-9)
  - Alphabetic (upper and lower case)
  - Special characters (punctuation marks, bareckets)
  - Control characters (used by equipments on both ends of the link to control data flow
- Data code:
  - ASCII
  - EBCDIC

CODE

$b_7 b_6 b_5$ → / Bits	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b_4 b_3 b_2 b_1 ↓ / Column → / Row	0	1	2	3	4	5	6	7
0 0 0 0	0	NUL	DLE	SP	0	@	P	`	p
0 0 0 1	1	SOH	DC1	!	1	A	Q	a	q
0 0 1 0	2	STX	DC 2	"	2	B	R	b	r
0 0 1 1	3	E TX	gC 3	#	3	C	S	c	s
0 1 0 0	4	EOY	DC 4	$	4	D	T	d	t
0 1 0 1	5	ENQ	NAK	%	5	E	U	e	u
0 1 1 0	6	ACK	SYN	&	6	F	V	f	v
0 1 1 1	7	8E L	E T8	'	7	G	W	g	w
1 0 0 0	8	BS	CAN	(	8	H	X	h	x
1 0 0 1	9	HT	EM	)	9	I	Y	i	y
1 0 1 0	IO	LF	SUB	*	:	J	Z	j	z
1 0 1 1	11	VT	ESC	+	;	K	[	k	{
1 1 0 0	12	FF	rs	,	<	L	\	l	|
1 1 0 1	13	CR	GS	-	=	M	]	m	}
1 1 1 0	14	SO	RS	.	>	N	^	n	~
1 1 1 1	15	S1	US	/	?	O	_	o	DEL

Parity bits for error checking

Data	Odd Parity added	Even Parity added
1001011	10010111	10010110
0010101	00101010	00101011

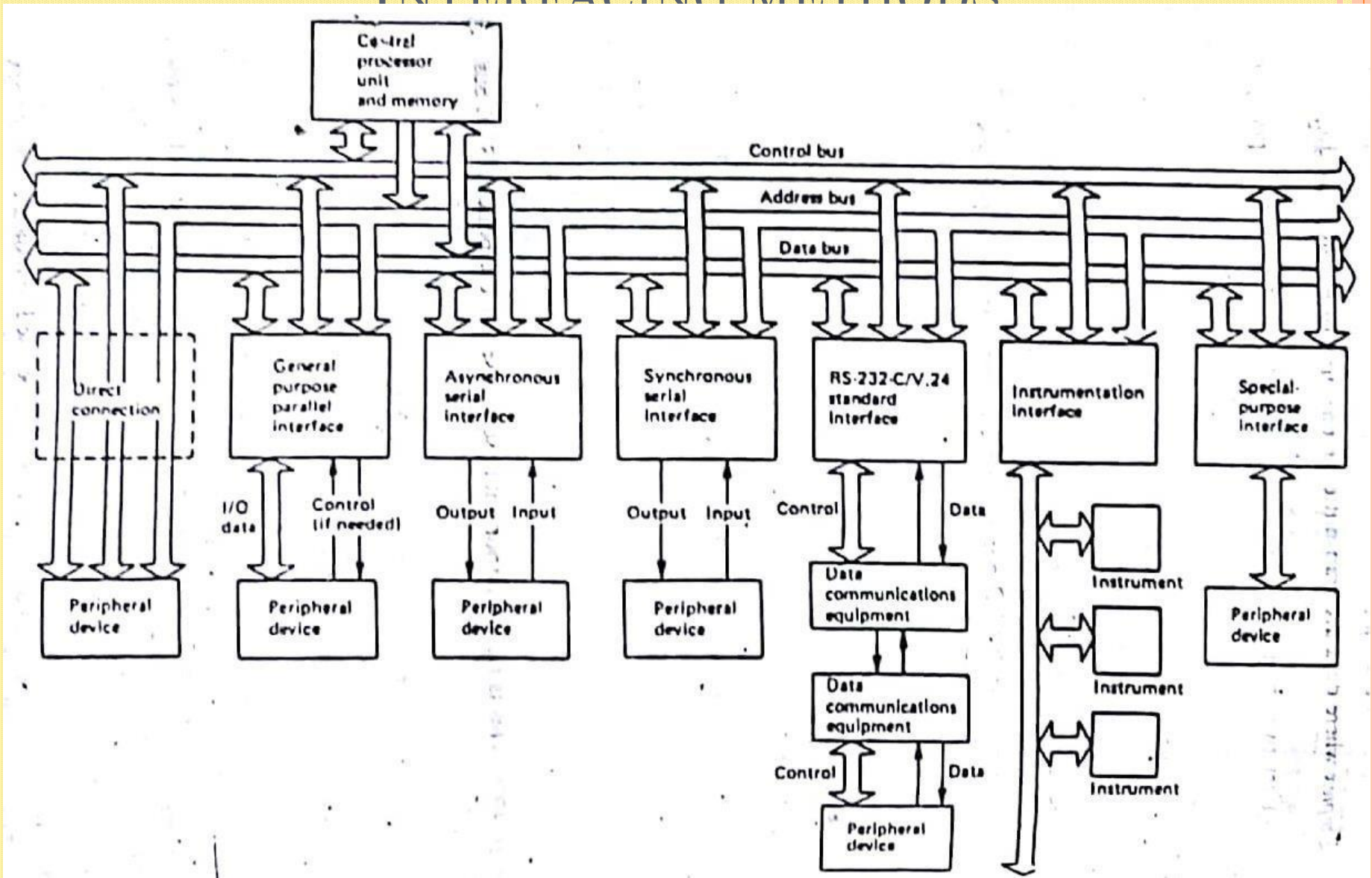
Interfacing methods

- Duplex
  - Full duplex
  - Half-Duplex
  - Simplex

Range of methods

- Direct Connection
  - Direct connections
  - General Purpose parallel interface
  - Asynchronous serial interface
  - Synchronous serial interface
  - RS 232 –C/V
  - IEEE 488
  - Special purpose interfaces

INTERFACING METHODS



Week 9

- **Data Lines**

  The eight data lines, DIO1 through DIO8, carry both data and command messages.

  The state of the Attention (ATN) line determines whether the information is data or commands. All commands and most data use the 7-bit ASCII or ISO code set, in which case the eighth bit, DIO8, is either unused or used for parity.

- **Handshake Lines**

  Three lines **asynchronously** control the transfer of message bytes between devices. The process is called a **3-wire interlocked handshake**. It guarantees that message bytes on the data lines are sent and received without transmission error.

- NRFD (not ready for data) - Indicates when a device is ready or not ready to receive a message byte. The line is driven by all devices when receiving commands, by Listeners when receiving data messages, and by the Talker when enabling the HS488 protocol.
- NDAC (not data accepted) - Indicates when a device has or has not accepted a message byte. The line is driven by all devices when receiving commands, and by Listeners when receiving data messages.
- DAV (data valid) - Tells when the signals on the data lines are stable (valid) and can be accepted safely by devices. The Controller drives DAV when sending commands, and the Talker drives DAV when sending data messages.

- **Interface Management Lines**

Five lines manage the flow of information across the interface:

- ATN (attention) - The Controller drives ATN true when it uses the data lines to send commands, and drives ATN false when a Talker can send data messages.
- IFC (interface clear) - The System Controller drives the IFC line to initialize the bus.
- REN (remote enable) - The System Controller drives the REN line, which is used to place devices in remote or local program mode.
- SRQ (service request) - Any device can drive the SRQ line to asynchronously request service from the Controller.
- EOI (end or identify) - The EOI line has two purposes - The Talker uses the EOI line to mark the end of a message string, and the Controller uses the EOI line to tell devices to identify their response in a parallel poll.

Line Drivers and Line Receivers

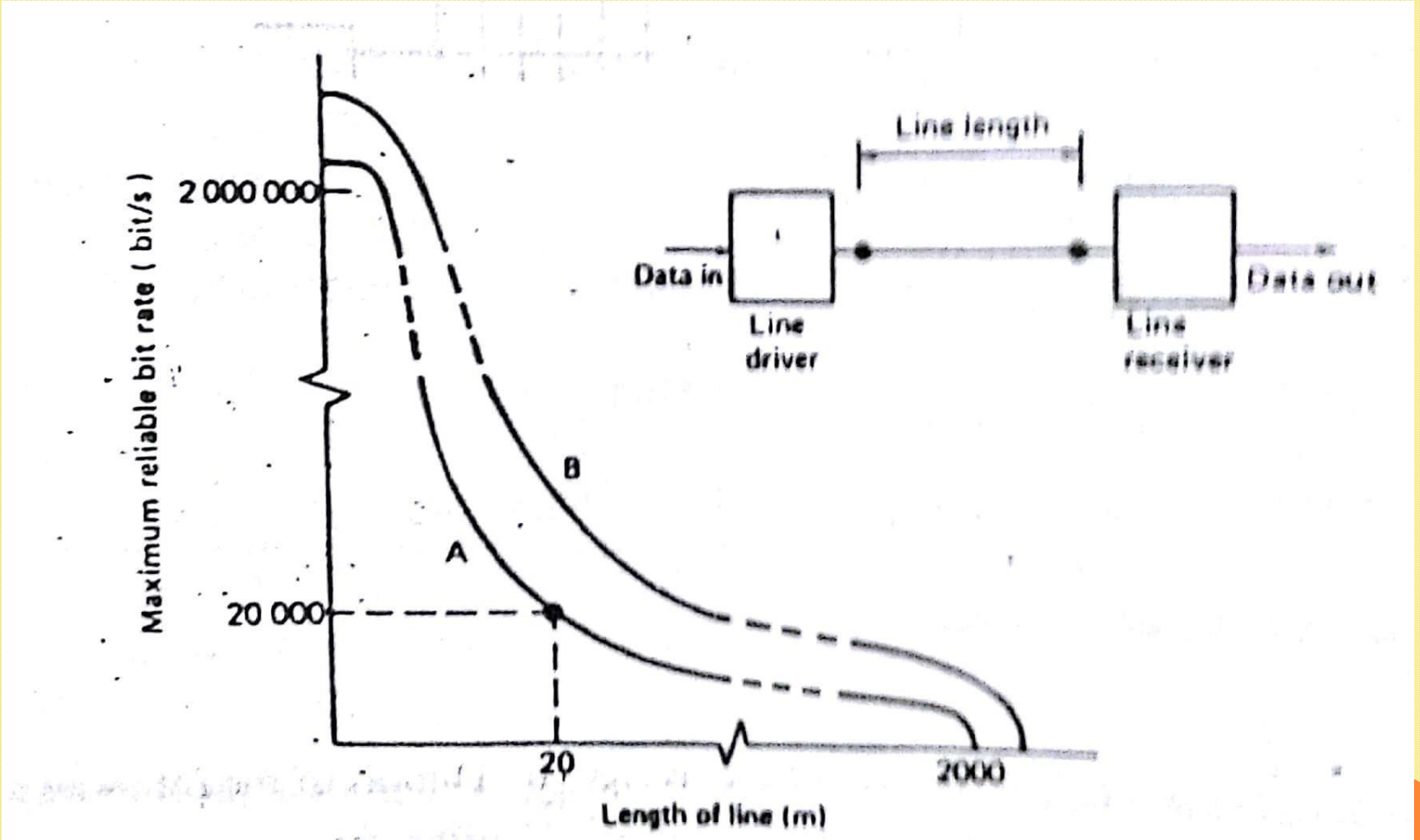


Figure 2.19 Maximum bit-rate versus line length.

Single ended line driver and receiver

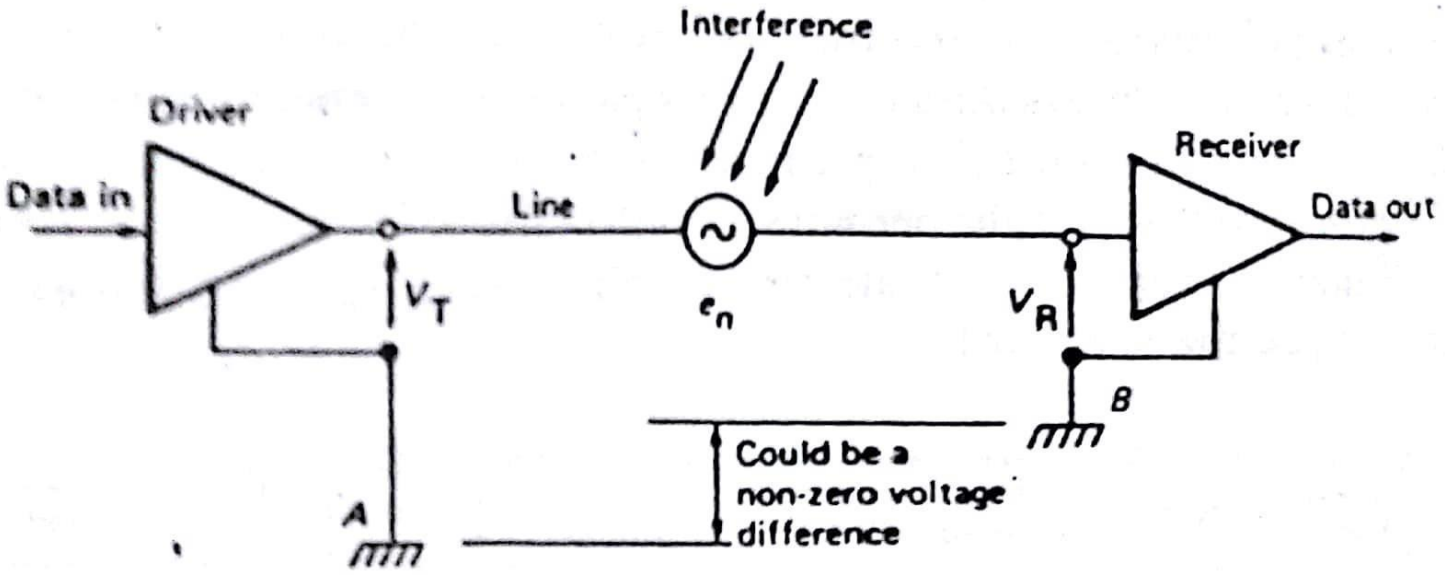


Figure 2.20 Single-ended line driver and receiver.

Differential line receciver

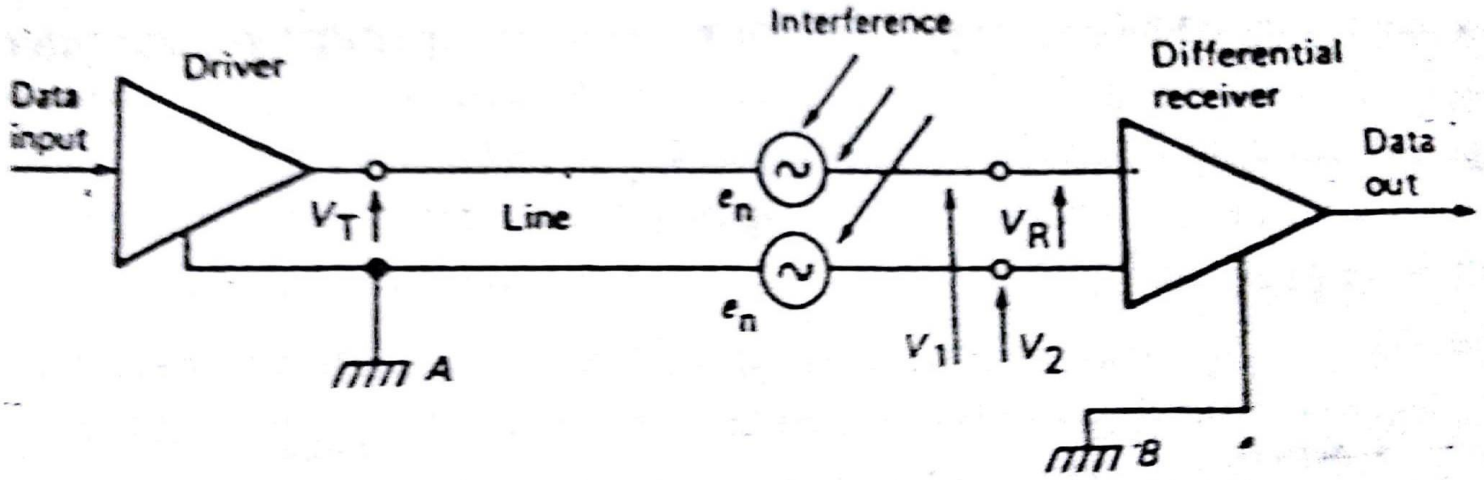


Figure 2.23 Differential line receiver.

Balanced driver and differential line receiver

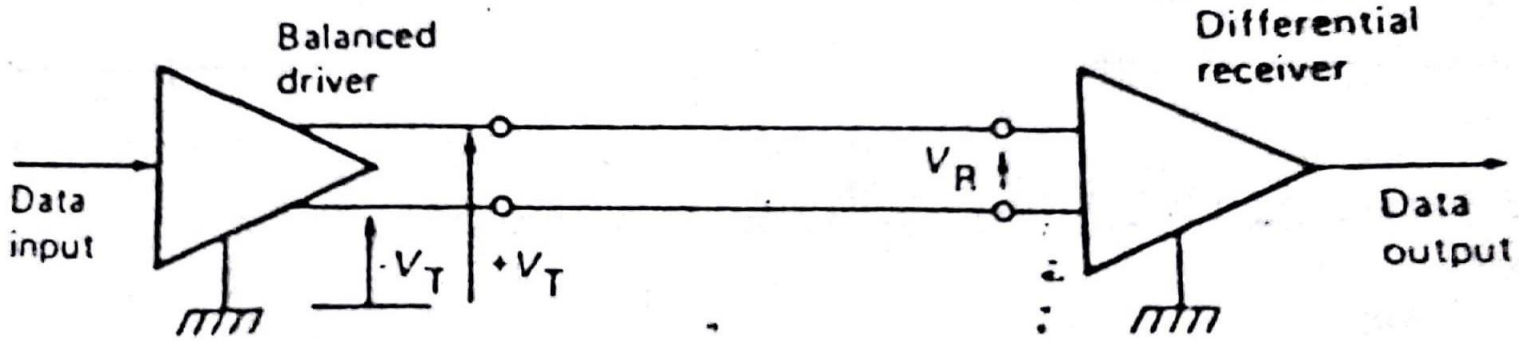


Figure 2.24 Balanced driver and differential line receiver.

Optical fiber cable

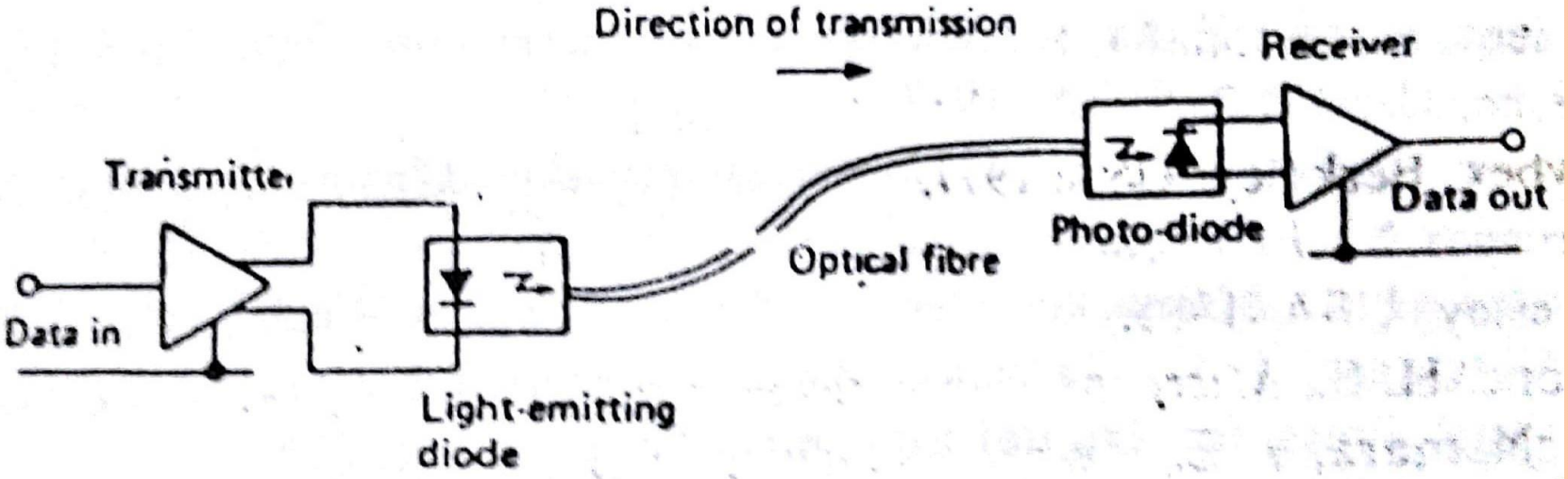


Figure 2.26 Optical-fibre arrangement.

Week 10

Memories

- Memories are devices into which information can be written to and retrieved whenever required.

- Types of Memories:
  - ROM
  - RAM

ROM AND ROM

- M
- PROM
- EPROM
- EEPROM
- h ROM

- RAM
- SRAM
- BSRAM
- DRAM
- FPM DRAM
- Enhanced RAM
- EDO DRAM
- BEDO DRAM
- NVRAM
- SDRAM
- DDR DRAM
- DRDRAM

ROM

- Read Only Memory
- Non volatile
- Once programmed, it is permanent and not reversible
- It is developed by manufacturers and not programmed by the users.
- ROMs are cheap compared to other types of read only memories

PROM

- Programmable ROM
- One time programmable by the user
- Useful for prototyping purpose
- 27PC32 (4k X 8), 27PC010 (128k X 8)

EPROM

- Erasable PROM
- Has a window on the chip
- Once programmed, it cannot be exposed to sunlight
- When wants to rewrite, the window should be exposed to sunlight for 5 to 10 minutes and the data is erased
- then it can be programmed again separately and can be plugged into the

EEPROM

- Electrically Erasable PROM
- It can be programmed in-circuit
- No window like EPROM
- A single bitcan be erased and write it again while on-board
- Eachlocation can be rewritten 10000 times
- Programming EEPROM takes more time than reading, so it cannot replace RAM
- 28C84 (8kX 8)

Flash ROM

- Similar to EEPROM but has fixed block sizes (128-512 k bits) which can be erased at a time
- Instead of each bit, entire block can be erased and rewritten
- 28F256 (32k X 8), 28F032 (2M X 16 or 4M X 8)
- Higher capacity flash memories available known as Pen drive or memory stick

RAM

- Random Access Memory
- Read and write operation and volatile
- Two types
  - SRAM (static RAM)
  - DRAM (Dynamic RAM)

SRAM

- Uses flip-flop as basic cell to store one bit
- Available in bipolar and MOS technology
- Costly compared to DRAM
- Takes four times of space than DRAM for a given number of bits
- Faster access time than DRAM
- 25 ns access time compared to 60 ns access time for DRAM
- For level-1 and level-2 cache, SRAM are preferrable
- 265k X 16, 3.3V SRAM with access time of 15 ns available

BSRAM

- BURST (or SYNCHBURST) SRAM
- SRAMs synchronized either with the system clock or the cache bus clock are known as Burst SRAM.
- This permits it to be more easily synchronized with any unit that accesses it and reduces the access waiting time.

DRAM

- Dynamic RAM
- Basic cell capacitor, that needs frequent charge refreshing.
- Higher density and less expensive than SRAM
- Uses MOS technology

Week 11

FPM DRAM

- Fast Page Mode DRAM
- In DRAM, the RAS (row address strobe) is first sent out with DRAM row address and this process selects the row of the DRAM
- Then CAS (column address strobe) is sent with column address to select the column and thus the cell.
- The state of the cell is sent out in the READ operation
- If the RAS signal is kept active and CAS is sent several times with different column addresses, all the row cells can be read. This mode is called Fast Page.
- This reduces access time and power requirements

EDRAM

- Enhanced DRAM
- A combination of SRAM (typically 256 bytes) and DRAM in a single package is known as EDRAM.
- Used for level-2 chache
- Data is read first from faster SRAM and if it is not there, it is read from DRAM

EDO RAM or EDO DRAM

- Extended Data Output RAM or DRAM
- It is similar to Fast Page Mode DRAM with additional feature of starting a new access cycle while maintaining the data output of the previous cycle.
- It creates a certain amount of overlap in operation resulting improved speed.
- Its 5% faster than FPM DRAM and 25% faster than standard DRAM

BEDO DRAM

- Burst Extended Data Output DRAM
- It can send out data from one READ operation while at the same time it would be reading the address of the next data to be sent.
- Also, after reading the address, it can send the data in three successive clock cycles without clock coordination, that is, three successive outputs seem to be sent from the RAM in a sudden burst.

NVRAM

- Non Volatile RAM or Shadow RAM
- When power is on, it works like a RAM but the moment it falls below +5V, it transfers everything to the shadow EEPROM. When power comes back, the reverse process is done and the contents are transferred back to RAM.
- Cost is too high, so its obsolete now.

SDRAM

- Synchronous DRAM
- Synchronized with the clock speed that the system bus is optimized for.
- The speed is specified in MHz rather than in ns. This makes it easier to compare bus speed and the RAM chip speed.

DDR DRAM

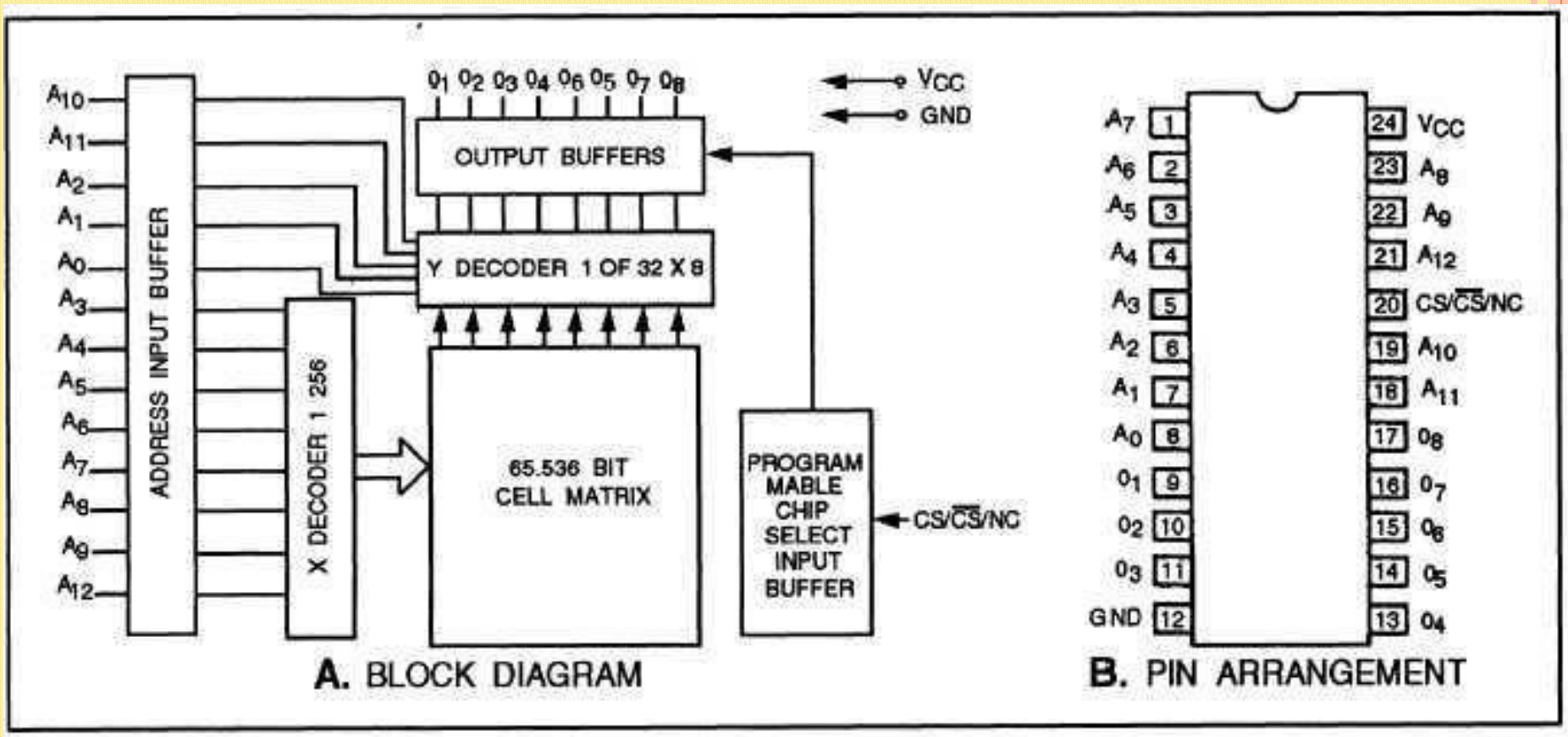
- Double Data Rate Synchronous DRAM
- High speed memory as they use both rising and falling edges of the clock signal to transfer data.
- A computer system with clock of 133 MHz running DDR SDRAM will perform like a 266 MHz machine.
- DDR 1 is the 1st generation of DDR family – highest speed 400 MHz
- DDR 2 is the 2nd generation of DDR family – starts with 400 MHz as lowest speed
- DDR3 is the 3rd generation of DDR family - bus speed upto 2000 MHz.

TABL9 8.1 DRAM Technologies

i DYN.1MIG RTU! @RAM1 $IE›VORY TECHNO I!OGIE•$

Type	Year of Intro.	Maximum Clock Rate	Bus Width	Peak Bandwidth	Volts
FPV	1990	£51A1tz	64 bits	200 MBps	5v
EDO	1994	40MHz	64 bits	320 MBps	5v
''SDRAM	1996	J 33MHz	64 bits	1.1 GBps	3.3v
RDRAM	1998	400MHz (×2)	16 bits	800 MBps	2.5v
DDR SDRAM	2000	266MHz (×2)	64 bits	4.2 GBps	2.5v
DDR2	2003	f33MHz	64 bits	8.5 GBps	1.8v
J2DR3 SDRAM	2007	800MHz (x2)	64 bits	12.8 GBps	1.5v

ROM


A10
A11
A2
A1
A0
A3
A4
A5
A6
A7
A8
A9
A12
ADDRESS INPUT BUFFER
X DECODER 1 256
O1 O2 O3 O4 O6 O5 O7 O8
OUTPUT BUFFERS
Y DECODER 1 OF 32 X 8
65.536 BIT CELL MATRIX
PROGRAM MABLE CHIP SELECT INPUT BUFFER
VCC
GND
CS/CS/NC
A. BLOCK DIAGRAM
A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O1 9
O2 10
O3 11
GND 12
24 VCC
23 A8
22 A9
21 A12
20 CS/CS/NC
19 A10
18 A11
17 O8
16 O7
15 O6
14 O5
13 O4
B. PIN ARRANGEMENT
35NVM028

PROM

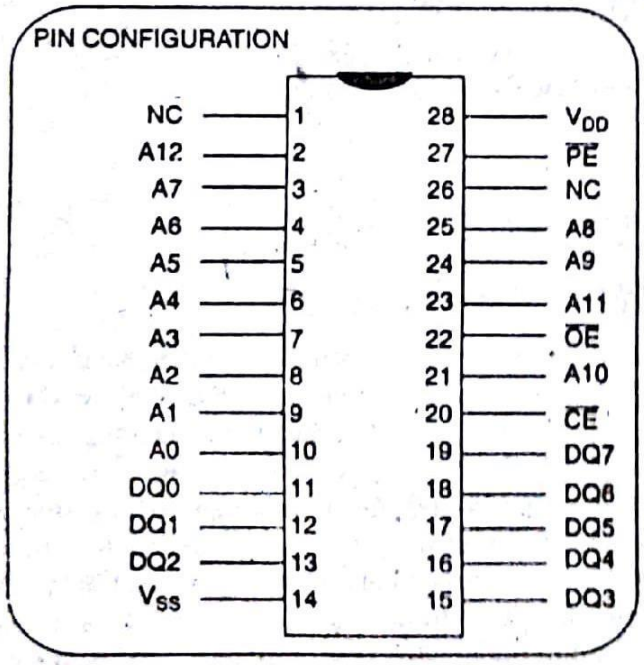


Fig. 8.1 (b) Block diagram of 8K × 8 PROM.

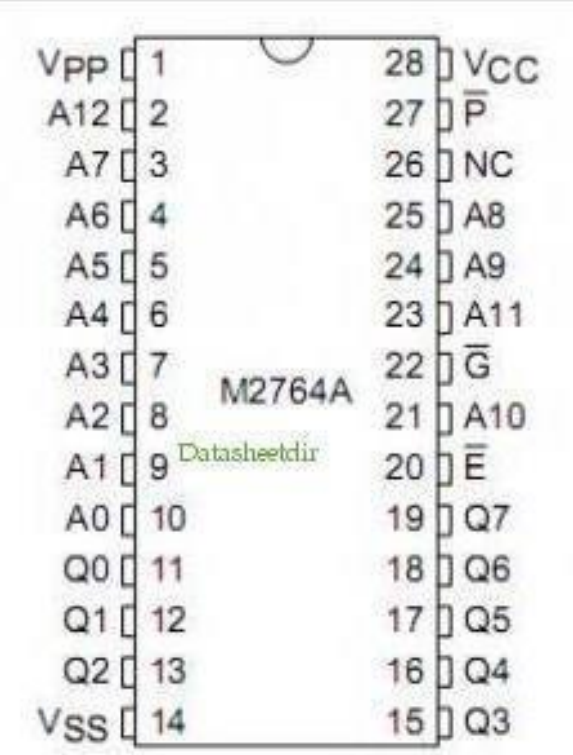
Table 1. Device Operation Truth Table[1]

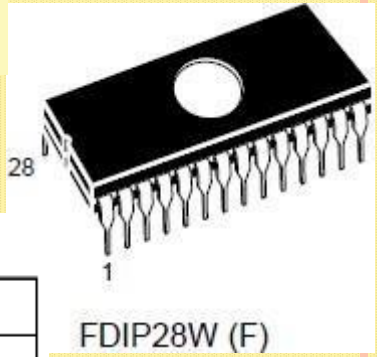
OE	*PE*	*CE*	*I/O MODE*	*MODE*
X	1	1	Three-state	Standby
0	1	0	Data Out	Read
1	0	0	Data In	Program
1	1	0	Three-state	Read[2]

Notes:
1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.

Week 12

EPROM(M2764A)





FDIP28W (F)

Signal Names

A0 - A12	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

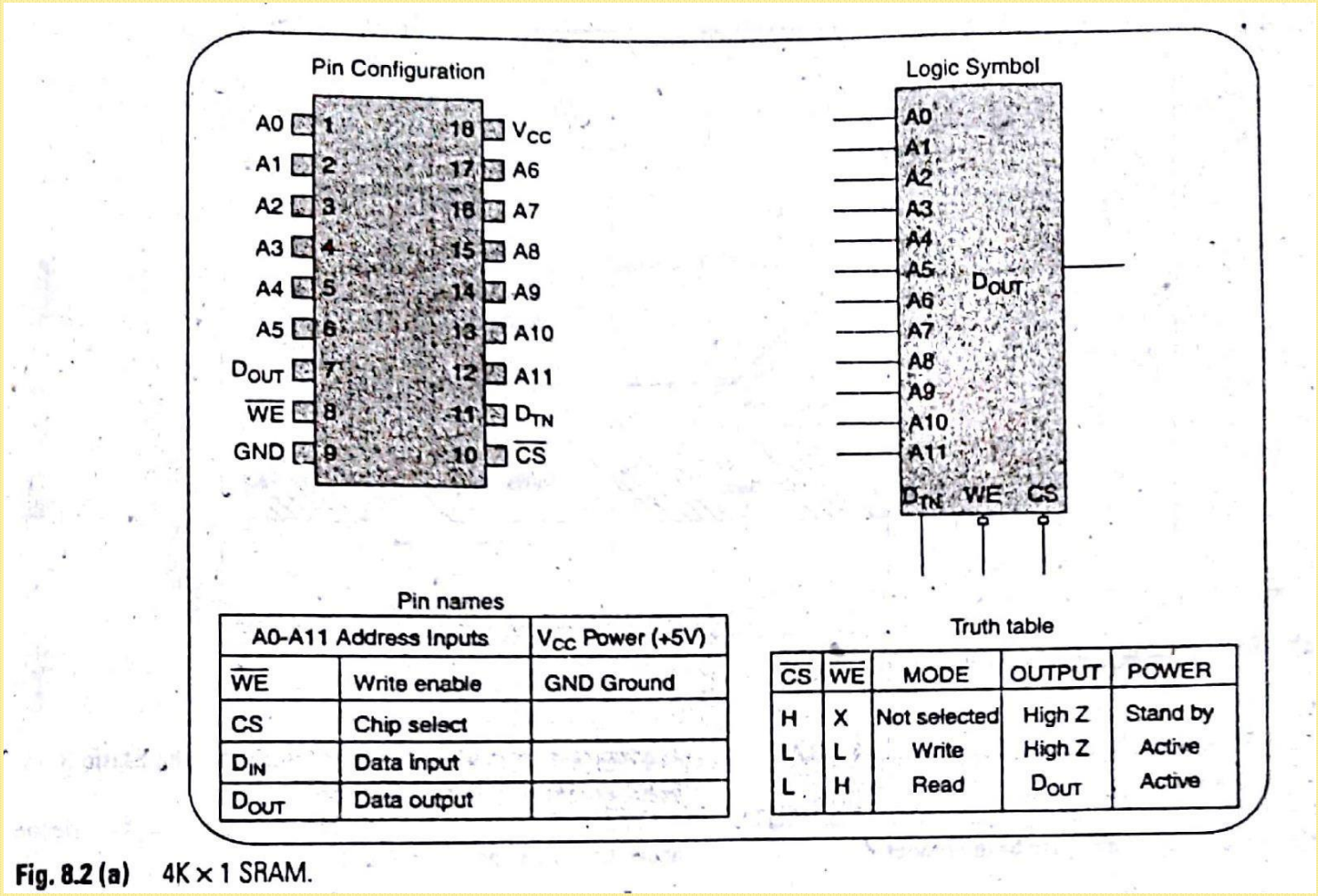
DESCRIPTION

The M2764A is a 65,536 bit UV erasable and electrically programmable memory EPROM. It is organized as 8,192 words by 8 bits.

The M27C64A is housed in a 28 pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

- FAST ACCESS TIME: 180ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 35mA max
- TTL COMPATIBLE DURING READ and PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE
- PROGRAMMING VOLTAGE: 12V

SRAM (4K X 1)



Pin names

A0-A11 Address Inputs		V_{CC} Power (+5V)
$\overline{WE}$	Write enable	GND Ground
CS	Chip select	
D_{IN}	Data input	
D_{OUT}	Data output	

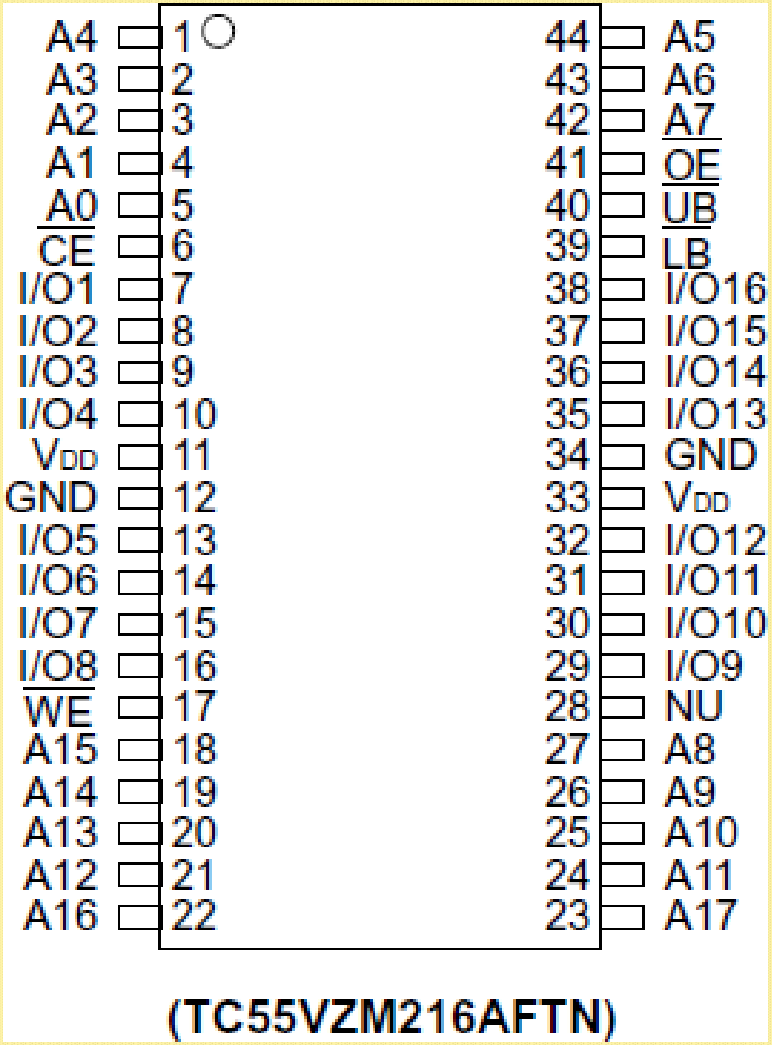
Truth table

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	Not selected	High Z	Stand by
L	L	Write	High Z	Active
L	H	Read	D_{OUT}	Active

Fig. 8.2 (a) 4K × 1 SRAM.

SRAM

262,144-WORD BY 16-BIT CMOS STATIC RAM

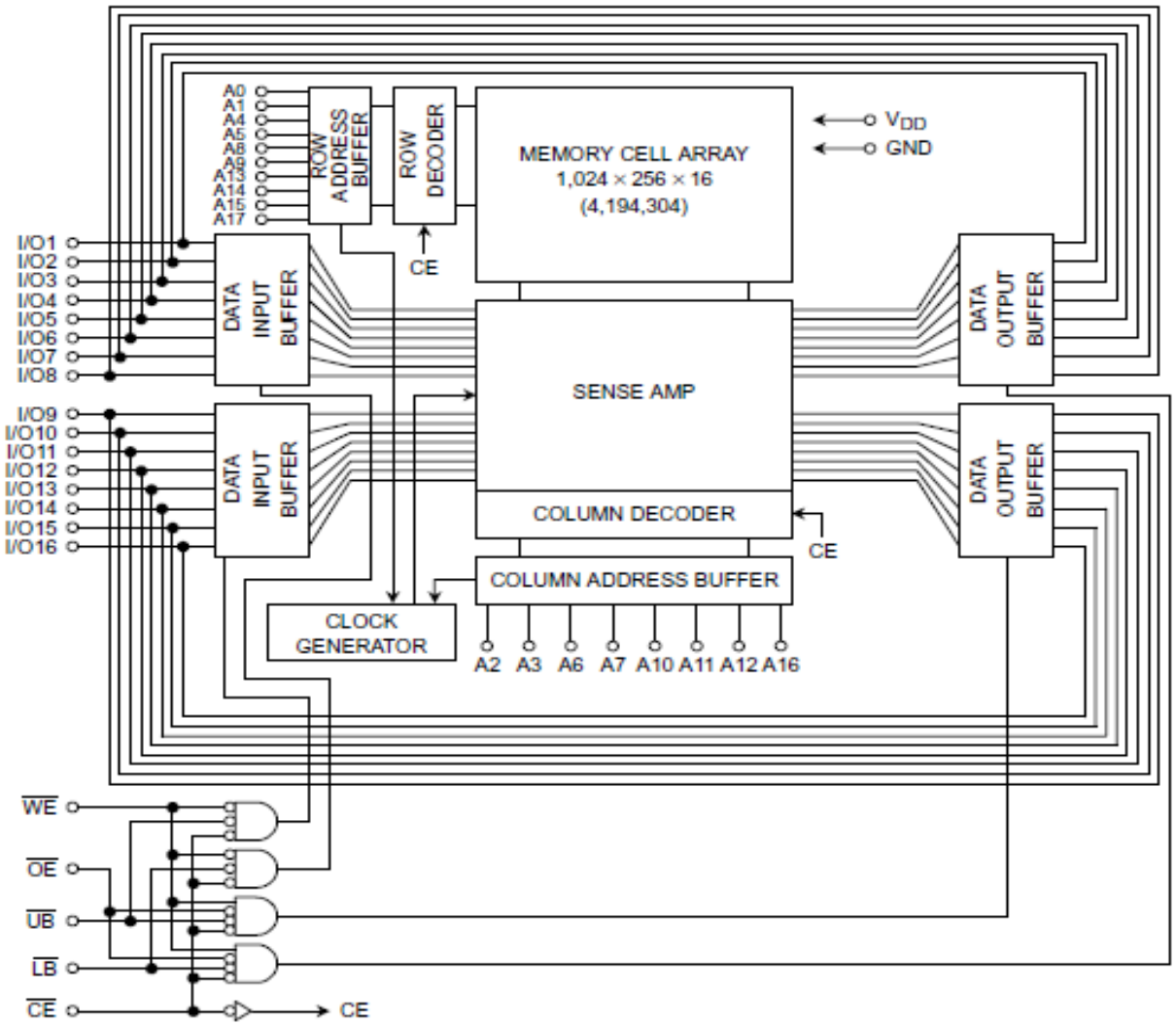


(TC55VZM216AFTN)

A0 to A17	Address Inputs
I/O1 to I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Inputs
V_{DD}	Power (+3.3 V)
GND	Ground
NU	Not Usable (Input)

SRAM

BLOCK DIAGRAM 262,144-WORD BY 16-BIT CMOS STATIC RAM



SRAM

262,144-WORD BY 16-BIT CMOS STATIC RAM

OPERATING MODE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1 to I/O8	I/O9 to I/O16	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High Impedance	Output	I_{DDO}
				L	H	Output	High Impedance	I_{DDO}
Write	L	*	L	L	L	Input	Input	I_{DDO}
				H	L	High Impedance	Input	I_{DDO}
				L	H	Input	High Impedance	I_{DDO}
Outputs Disable	L	H	H	*	*	High Impedance	High Impedance	I_{DDO}
	L	*	*	H	H			
Standby	H	*	*	*	*	High Impedance	High Impedance	I_{DDS}

* : Don't care

Note: The NU pin must be left unconnected or tied to GND.
You must not apply a voltage of more than 0.8 V to the NU.

Interfacing PROM and SRAM

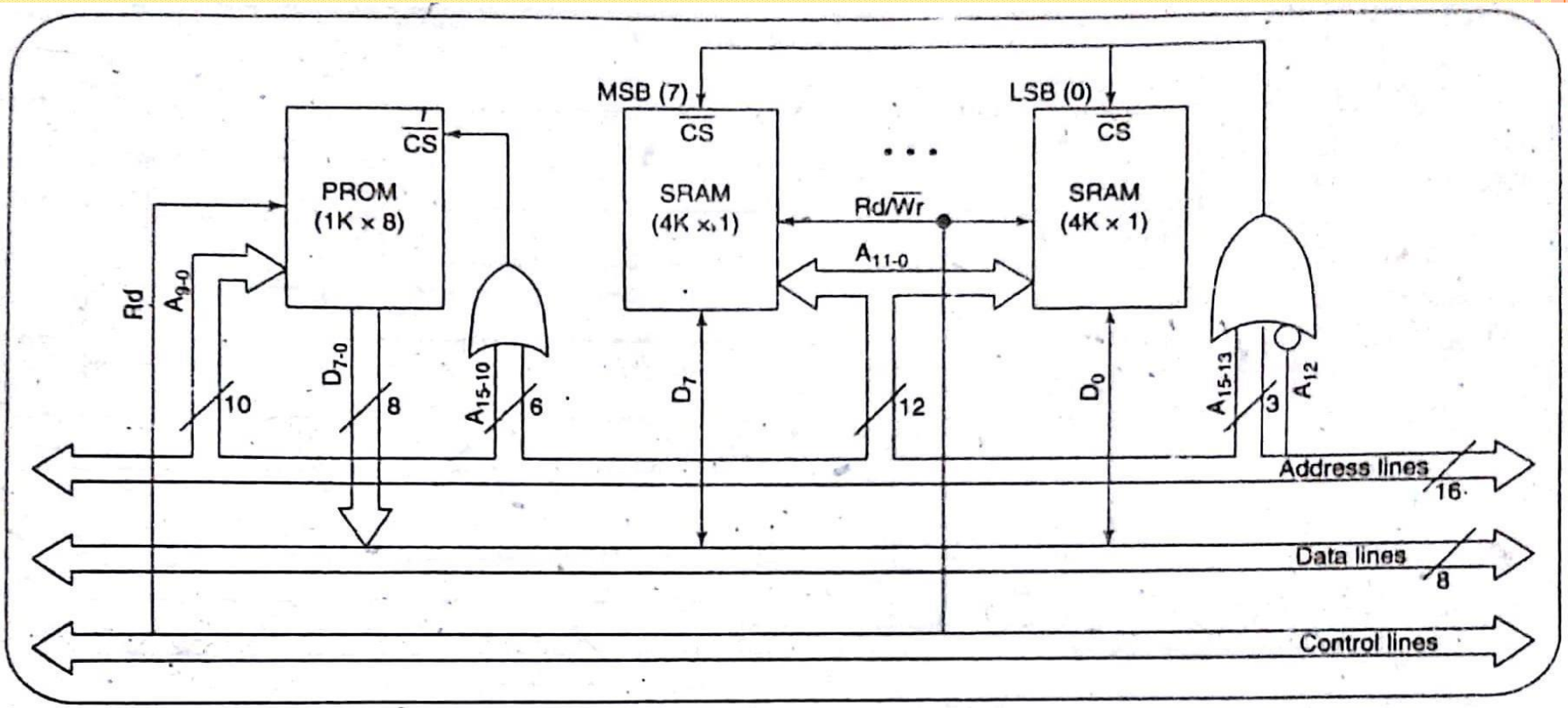


Fig. 8.3 Interfacing of PROM and SRAM to system bus.

DRAM Interfacing

- The basic cell is capacitor with READ and WRITE circuits
- Need charge refreshing at specified time interval
- Usually each cell needs to be refreshed once in 2 to 4 ms.
- Density is high and cost is low compared to SRAM
- DRAM are used in the main memory

Refreshing DRAM

- Refreshing is done Row-wise.
- The refresh time specified by the manufacturer is divided by the number of rows and this time interval is the row refresh time.
- A timer in the DRAM controller indicates that the row refresh time interval is over.
- The DRAM controller, if not in the process of reading or writing at that time, sends the row address from an internal row address counter and issues only RAS to refresh that row.
- Then increment the row address counter
- On the expiry of the next row refresh time interval, the incremented row is refreshed.
- In this way, it refreshes the entire DRAM cells in the manufacturer specified refresh time.

DRAM Interfacing

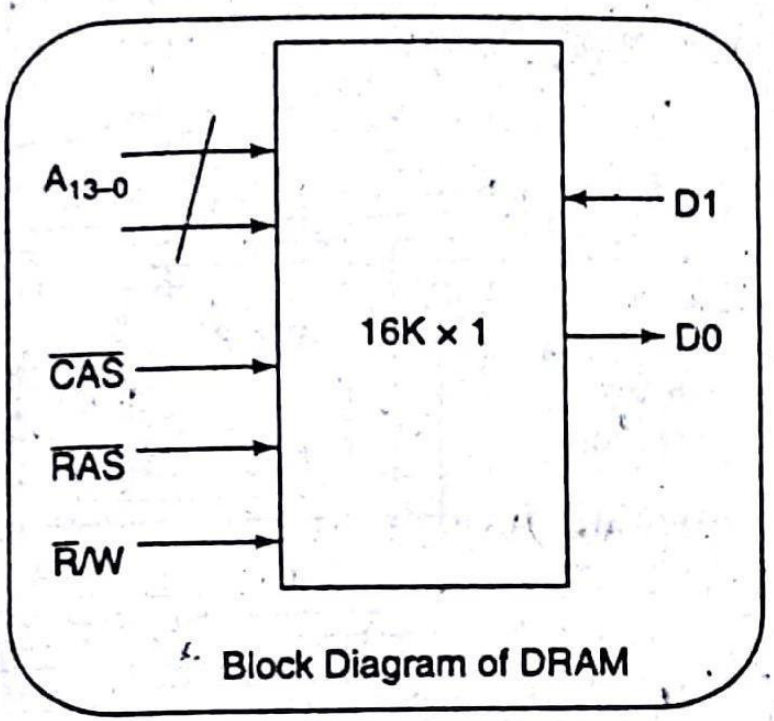


Fig. 8.5 16K x 1 DRAM.

Week 13

DRAM Controller

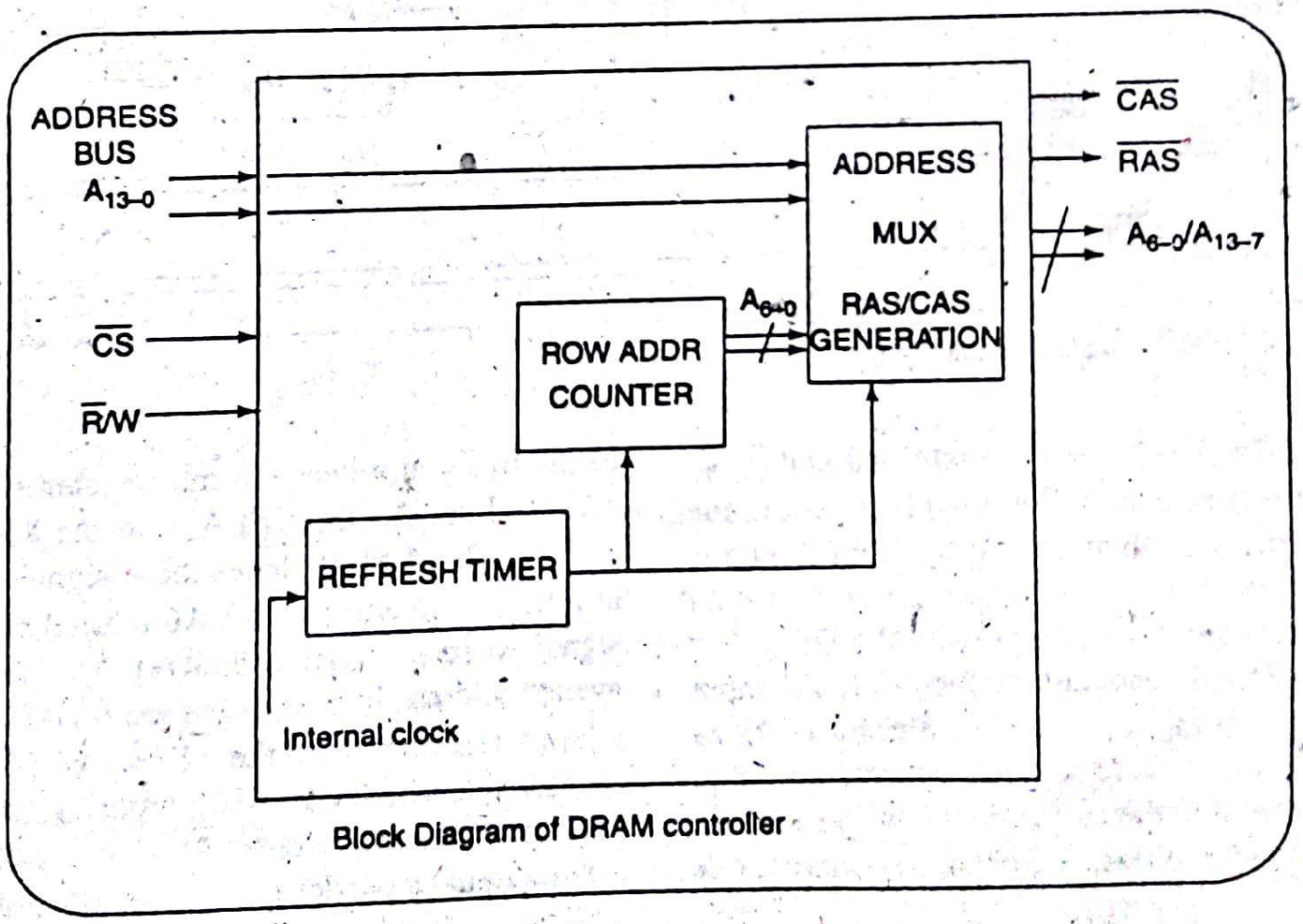


Fig. 8.6 Block diagram of DRAM controller.

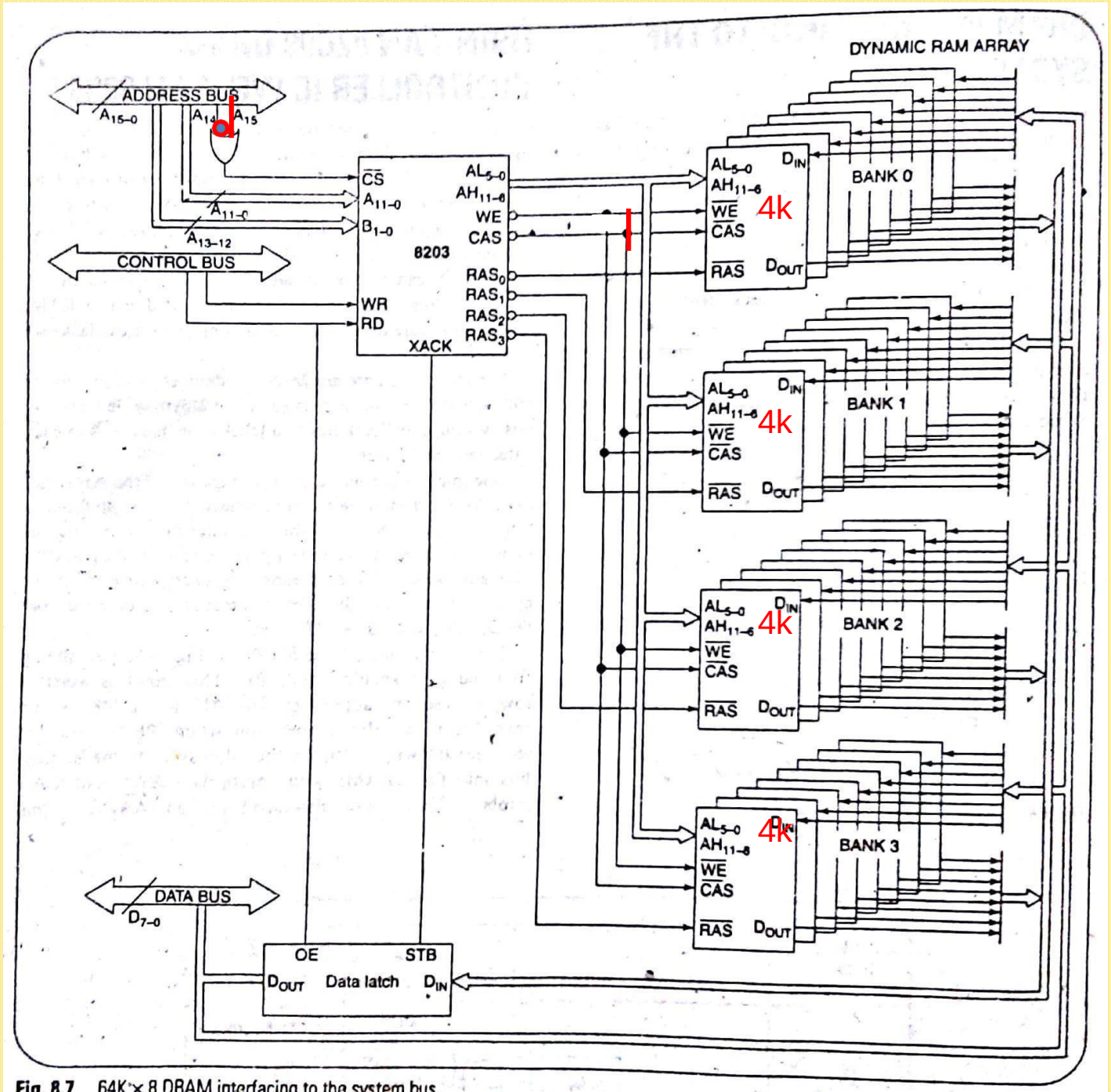


Fig. 8.7 64K × 8 DRAM interfacing to the system bus.

Error detecting and correcting in DRAM arrays

- Two types of error in DRAM:
  - Hard errors- due to permanent device failure (manufacturing defect or simply random breakdown in the chip).
  - Soft errors- one time error that takes place due to a noise pulse in the system or an alpha particle or some kind of radiation causing the change to capacitance where the data bit is stored.
- As the size of the RAM increases, the chance of a hard or soft error also increases.

Parity Generation/Checking

- The simplest method for detecting an error os with parity bit
- If DRAM has 8 bits, it adds another bit as parity bit resulting a total 9 bits.
- A 74LS280 parity generator/checker circuit generates a parity bit for each byte and stores it in the ninth location as each byte is written to the memory.
- When 9 bits are read out, the overall parity is checked by the circuit. If the parity is not correct, an error signal is sent to microprocessor.
- Limitation:
  - Two errors in a data word may cancel each other
  - It does not tell which bit in the word is wrong

Error detecting and correcting circuits

- A T4AS632 error detecting and correcting device (EDAC) can be connected in the data path between a 32 bit microprocessor and 16 Mbyte DRAM main memory
- When a data word is sent from the microprocessor to the memory, it also goes to the EDAC.
- As the data word is read in by the EDAC, several encoding or check bits are generated and written in memory along with the data word.
- The number of encoding bits, k, required is determined by the size of the data word, M, and the degree of detection/correction needed.
- The total number of bits required for a data word M is equal to M+K. eg., 5 encoding bits are needed to detect and correct a single-bit error in a 16 bit word, so a total of 21 bits have to be stored for each 16 bit word.
- When the processor reads a data from a data word from memory, the data word and the check bits from the memory go to the EDAC. The EDAC calculates the check bits for the data read out from the memory and compare with the stored check bits.

Week 14

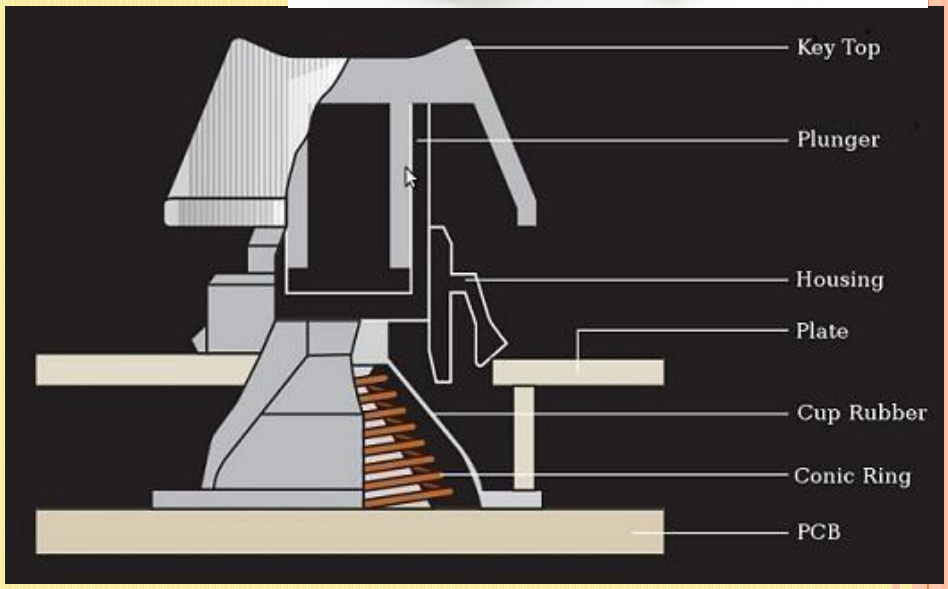
Interfacing with Keyboard

- Types of Keyboard
  - Mechanical Key switches
  - Membrane Key switches
  - Capacitive Key switches
  - Hall effect key switches

Mechanical Keyswitches

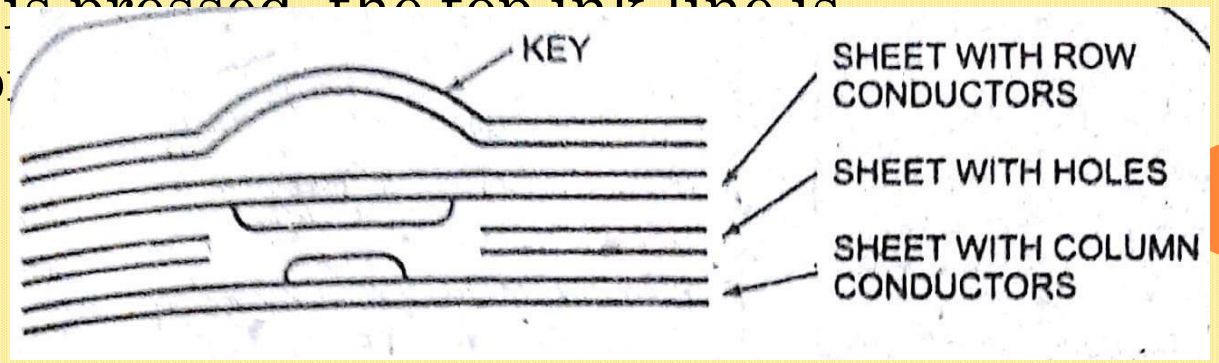
- Two pieces of metal pushed together when a key is pressed.
- Contact bounce
- Get oxidized or dirty
- Lifetime:

  1 million keystroke



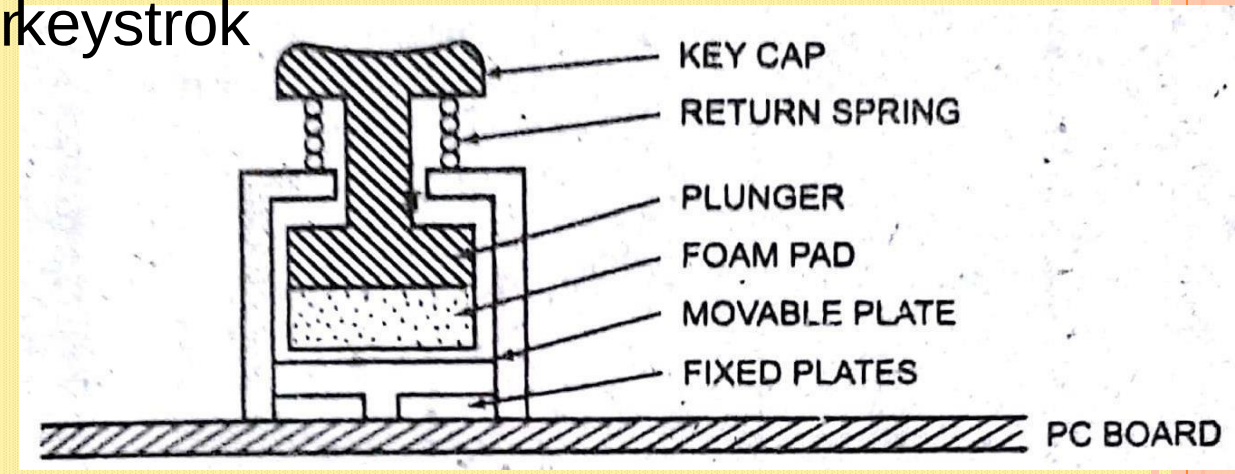
Membrane Keyswitch

- Special type of mechanical switch
- Consists of three layers of rubber or plastic sandwitch
- Top layer has a conducting line of silver ink running under each row of keys
- Middle layer has hole under each key position
- Bottom layer has a conducting line of silver ink running under each column.
- When a key is pressed, the top ink line is pushed to co



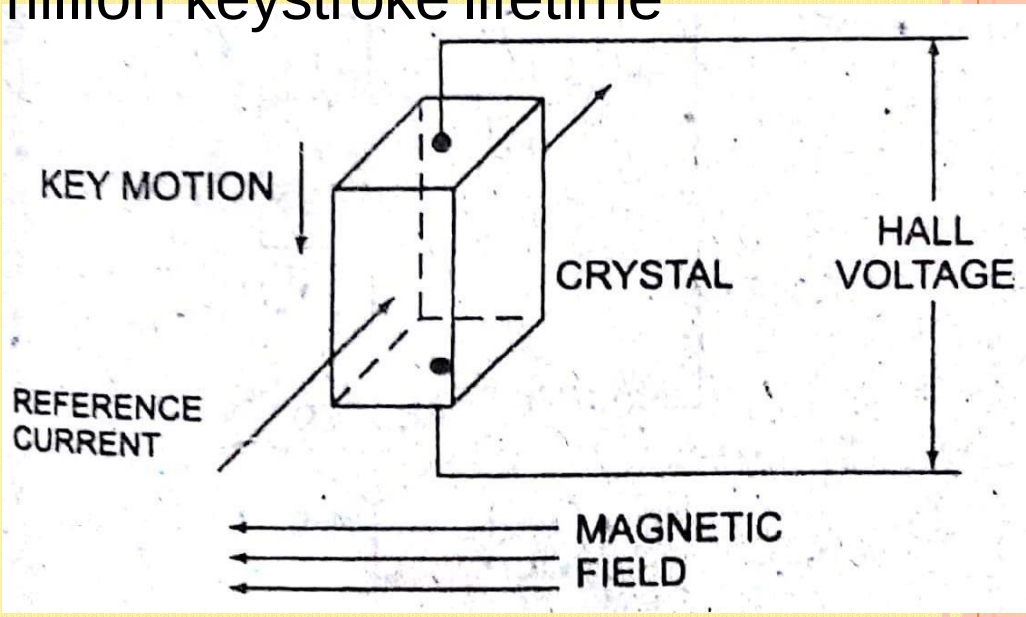
Capacitive Keyswitch

- Two metal plates
  - One movable and another fixed
  - When pressed, the movable plate is pushed closer to the fixed plate resulting change in capacitance
  - This change is detected by a circuit and produces a logic signal.
  - Main advantage: no physical contact
  - Lifetime: 20 millio keystrok



HALL EFFECT KEYSWITCH

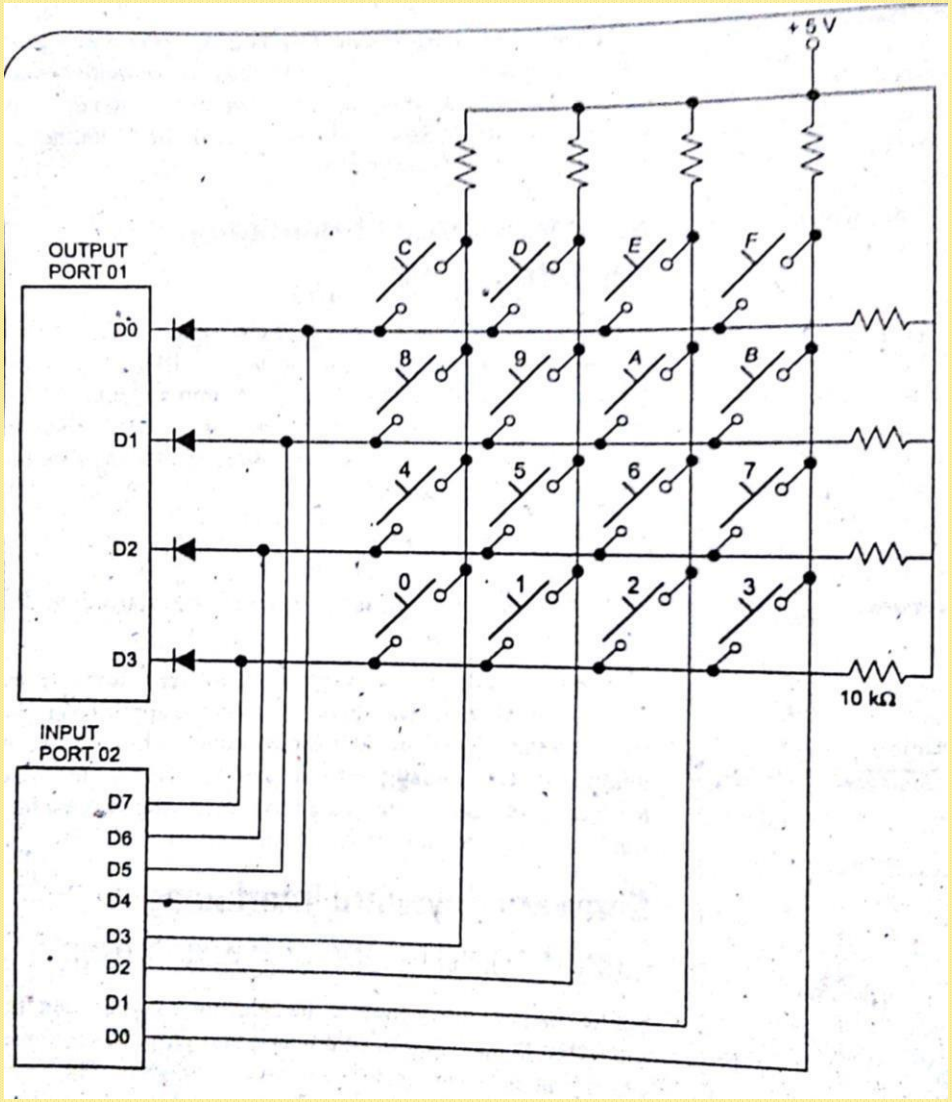
- A reference current is passed through a semiconductor crystal between two opposing faces.
- When a key is pressed, the crystal is moved through a magnetic field which has flux lines perpendicular to the current flow.
- It produces a small voltage called Hall voltage
- Very dependable and 100 million keystroke lifetime

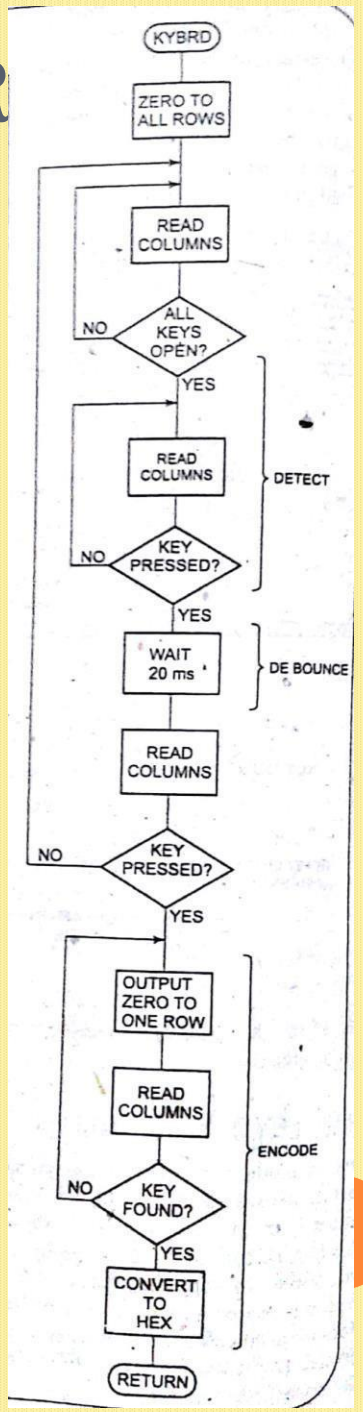


Keyboard Interfacing

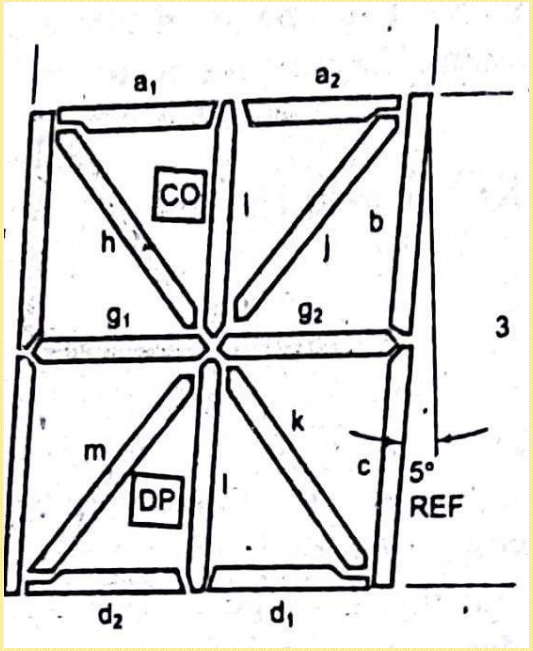
- Three steps to detect a keypress
  - Detect a keypress
  - Debounce the keypress
  - Encode the keypress

SOFTWARE KEYBOARD INTERFACING

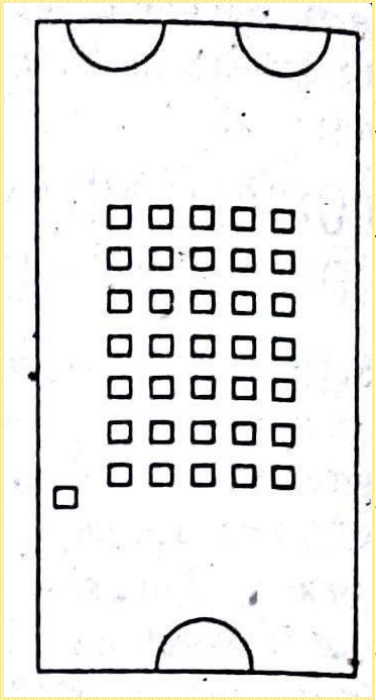




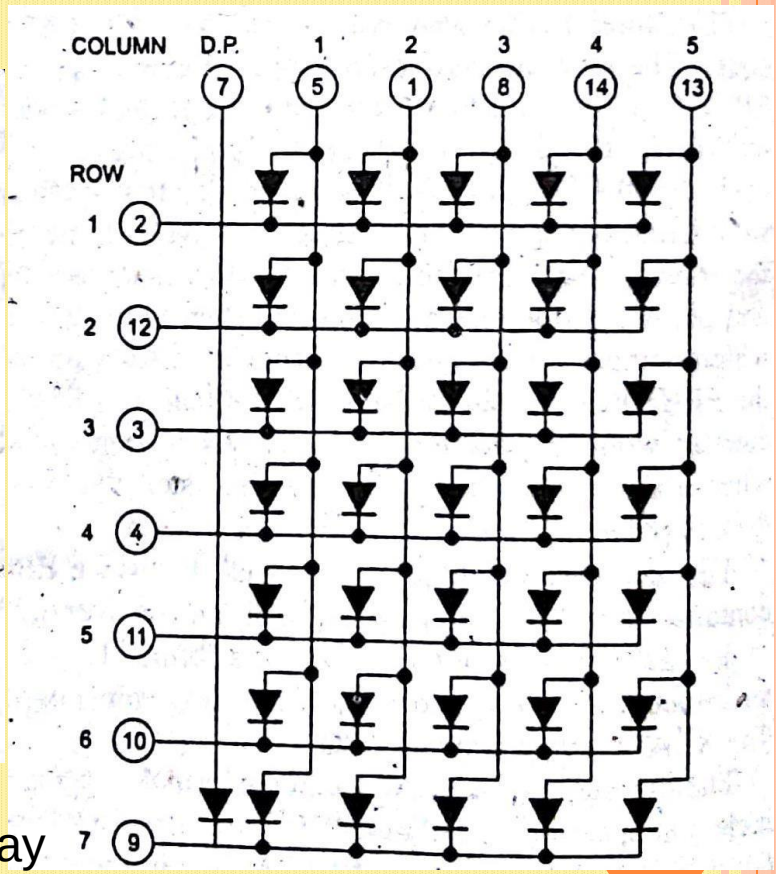
Interfacing to Alphanumeric Displays



18 segment display

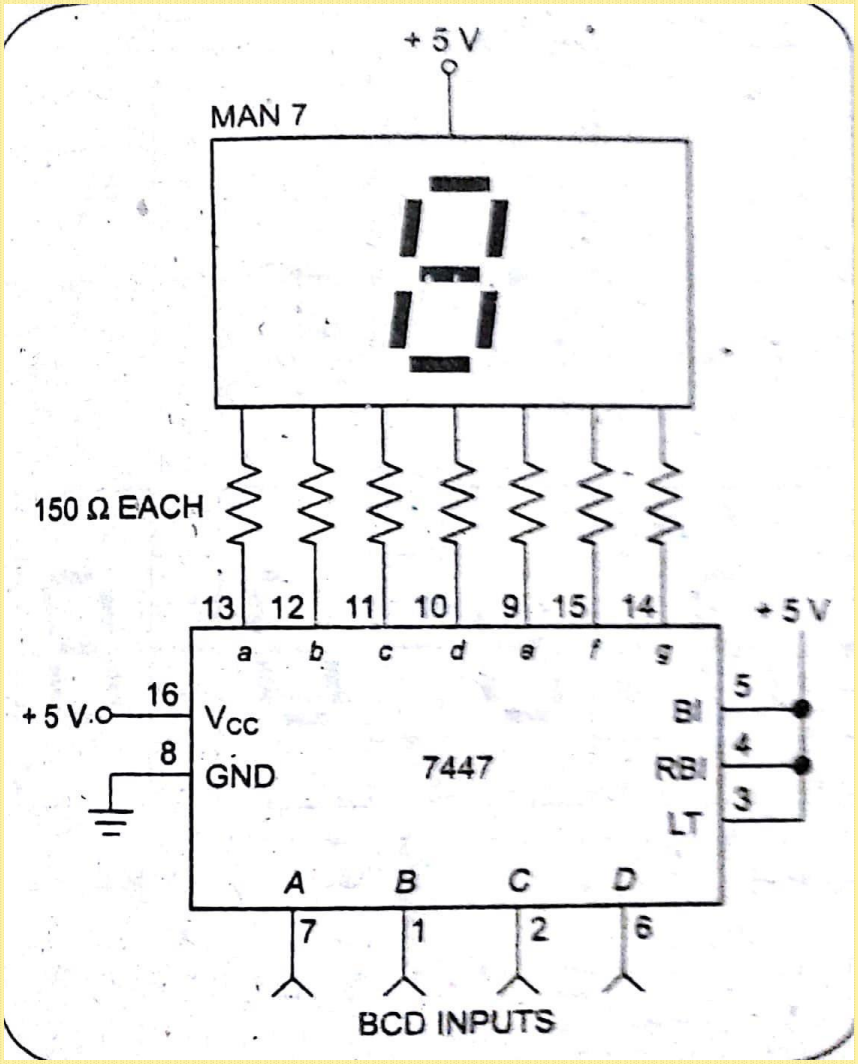


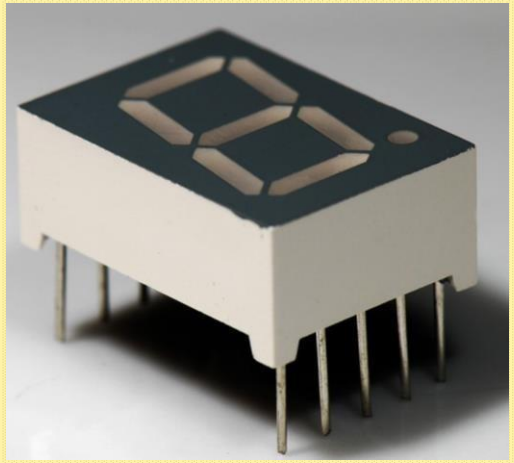
5 by 7 dot-matrix display

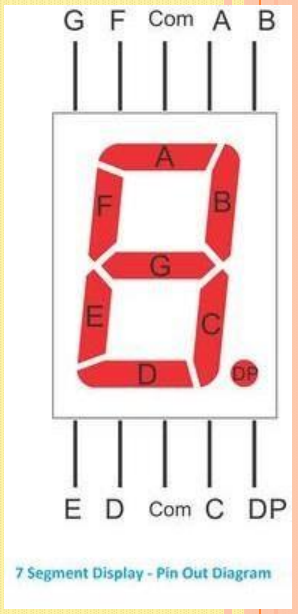


5 by 7 dot-matrix display

DIRECTLY DRIVING LED DISPLAY



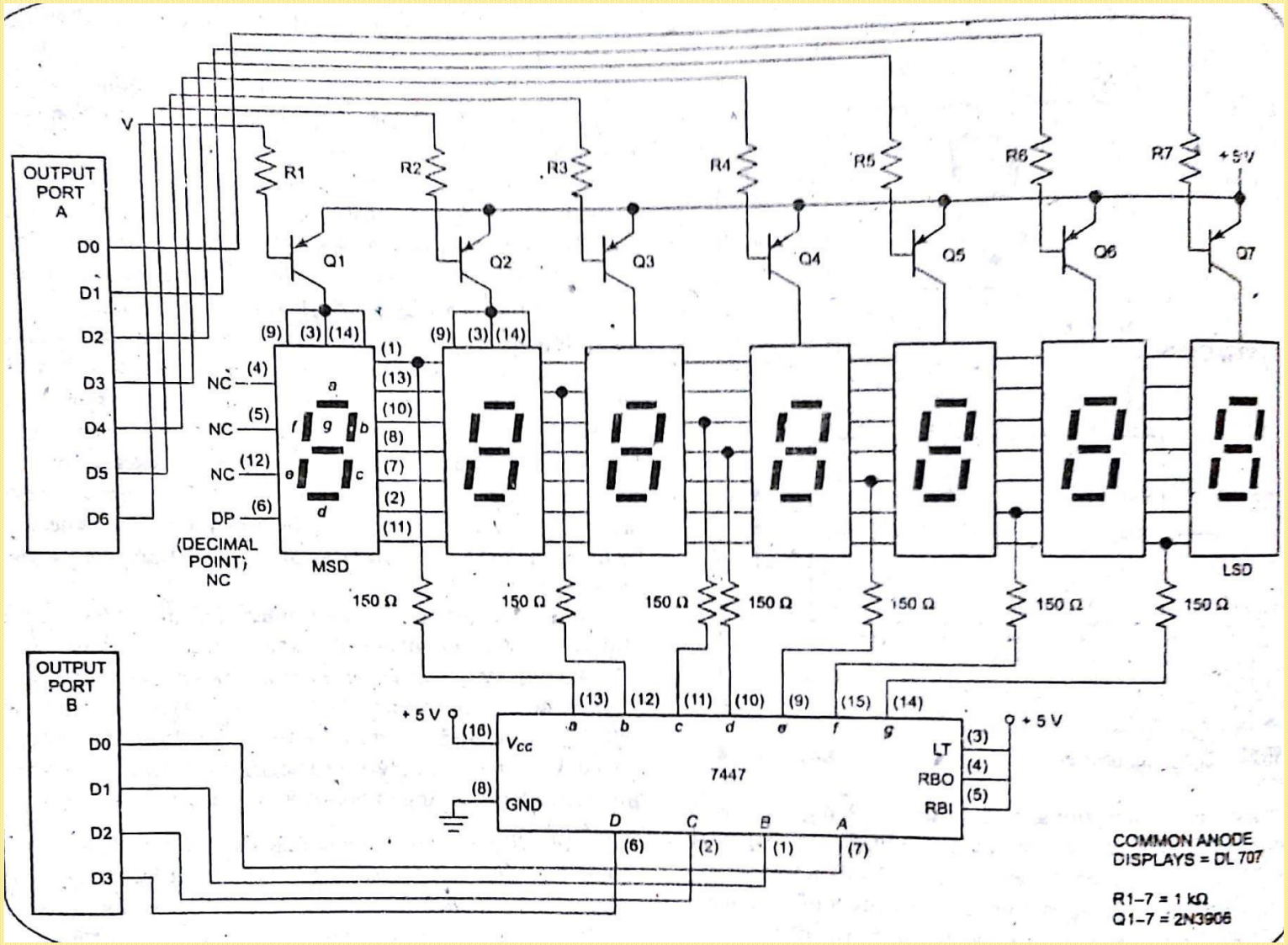




Binary Inputs				Decoder Outputs							7-Segment Display Outputs
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	1	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	0	1	1	1	1	1	6
0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	1	1	0	1	1	9

Week 15

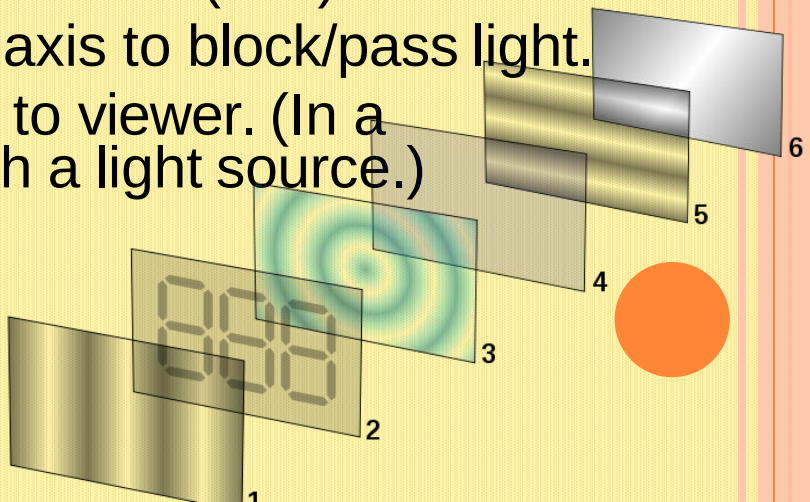
Software multiplexed LED displays


OUTPUT PORT A
D0
D1
D2
D3
D4
D5
D6
V
R1
R2
R3
R4
R5
R6
R7
+5V
Q1
Q2
Q3
Q4
Q5
Q6
Q7
NC
NC
NC
DP
(DECIMAL POINT) NC
MSD
LSD
150 Ω
OUTPUT PORT B
D0
D1
D2
D3
+5 V
Vcc
GND
7447
LT
RBO
RBI
D
C
B
A
COMMON ANODE DISPLAYS = DL 707
R1–7 = 1 kΩ
Q1–7 = 2N3906

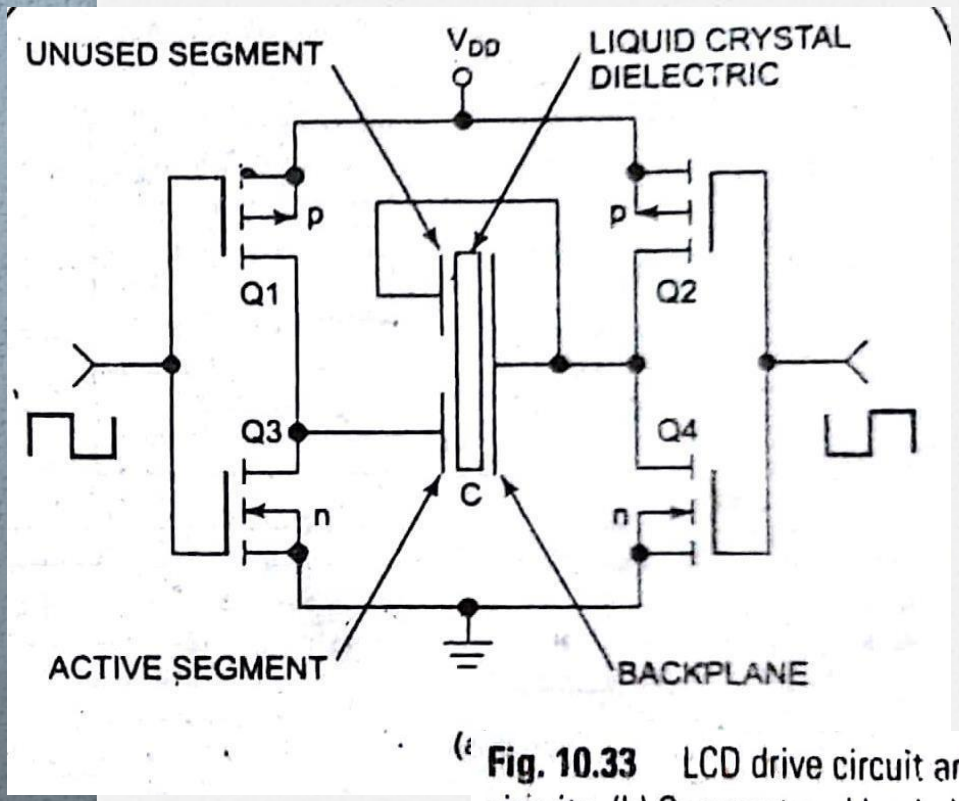
Liquid Crystal Display

Reflective twisted nematic liquid crystal display:

1. Polarizing filter film with a vertical axis to polarize light as it enters.
2. Glass substrate with ITO electrodes. The shapes of these electrodes will determine the shapes that will appear when the LCD is switched ON.
3. Twisted nematic liquid crystal. A **nematic liquid crystal** is a transparent or translucent liquid that causes the polarization of light waves to change as the waves pass through the liquid. When an electric field is applied, polarization does not occur.
4. Glass substrate with common electrode film (ITO).
5. Polarizing filter film with a horizontal axis to block/pass light.
6. Reflective surface to send light back to viewer. (In a backlit LCD, this layer is replaced with a light source.)



LCD display



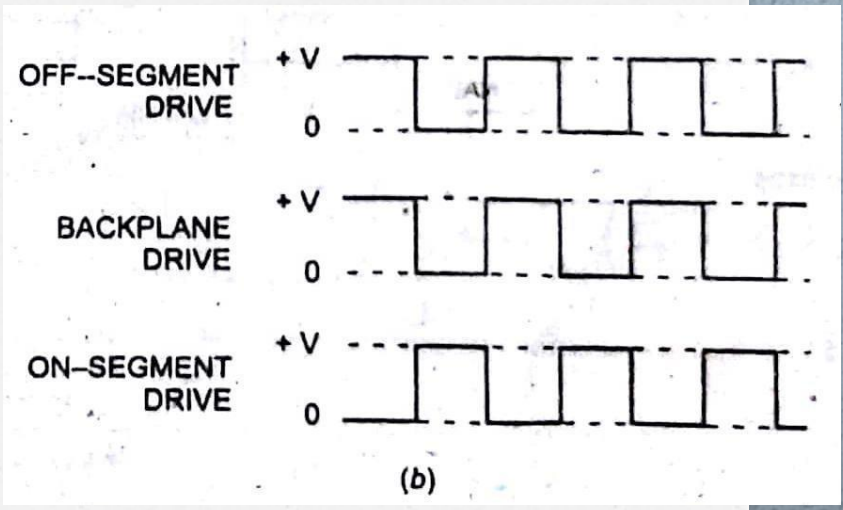


Fig. 10.33 LCD drive circuit and drive waveforms. (a) CMOS drive circuits, (b) Segment and backplane drive waveforms.

ICM 7211

ICM7211M, ICM7211AM
(PDIP)
TOP VIEW

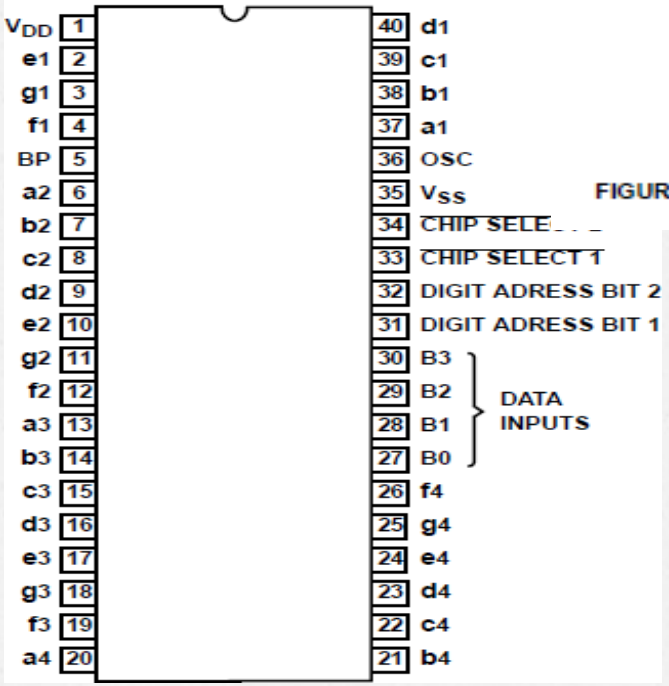


FIGURE 10. SEGMENT ASSIGNMENT

TABLE 1. OUTPUT CODES

BINARY				HEXADECIMAL ICM7211 ICM7211M	CODE B ICM7211A ICM7212AM
B3	B2	B1	BO		
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	BLANK

ICM7211M/ICM7212M Microprocessor In1erface Input Configuration

INPUT	DESCRIPTION	TERMINAL	CONDITIONS	FUNCTION
DA1	Digit Address Bit 1 (LSB)	31	V_{DD} = Logical One V_{SS} = Logical Zero	DA1 and DA2 serve as a 2-bit Digit Address Input DA2, DA1 = 00 selects D4 DA2, DA1 = 01 selects D3 DA2, DA1 = 10 selects D2 DA2, DA1 = 11 selects D1
DA2	Digit Address Bit 2 (MSB)	32	V_{DD} = Logical One V_{SS} = Logical Zero	
$\overline{CU}$	Chip Select 1	33	V_{DD} Inactive V_{SS} = Active	When both $\overline{CS1}$ and $\overline{CSz}$ are taken low, the data at the Data and Digit Select code inputs are written into the input latches. On the rising edge of either ~~chip select~~, the data is decoded and written into the output latches.
CS2	Chip Select 2	34	V_{DD} Inactive $V_{S:2}$ = Active	

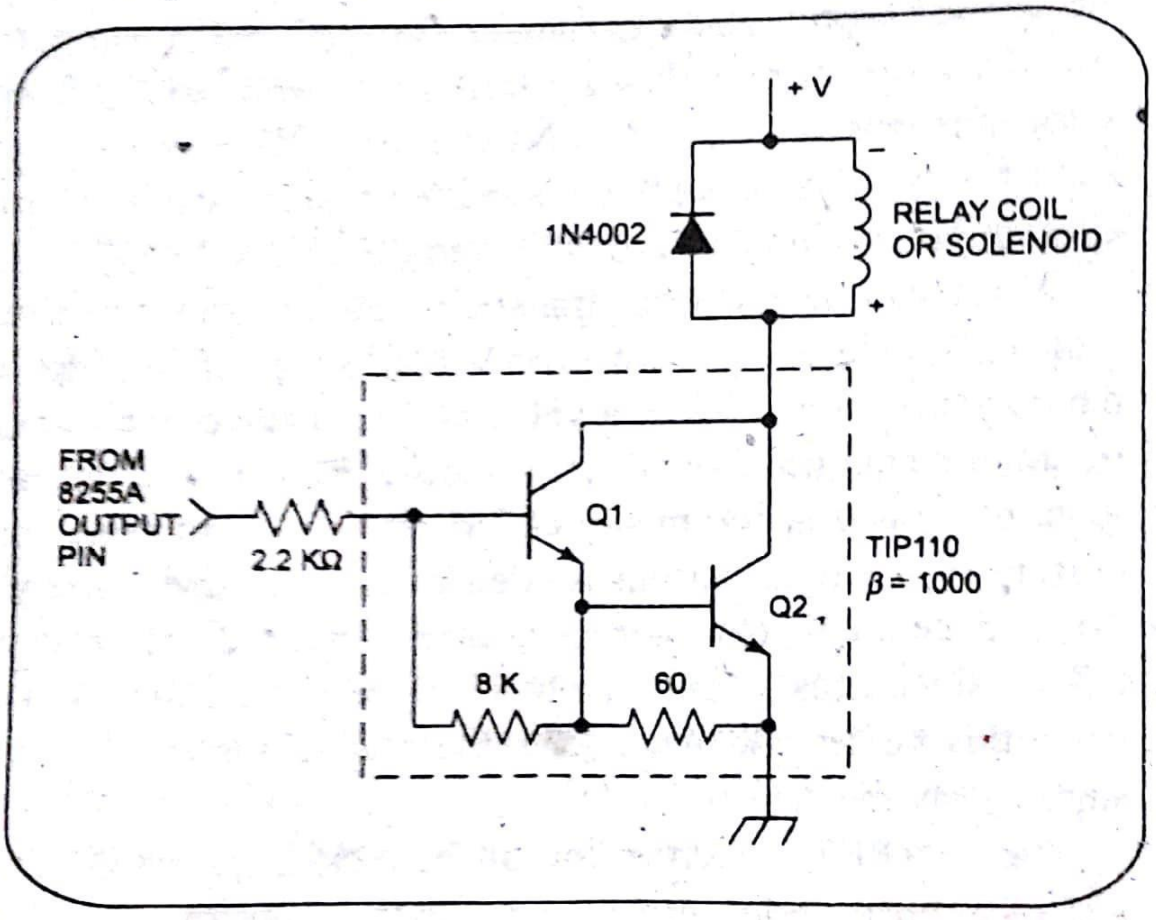


Fig. 10.36 Darlington transistor used to drive relay coil or solenoid.

Week 16

Printer

Types of printers

There are two types of printers

1. Impact Printers
2. Non-impact Printers

Impact Printers

An impact printer makes contact with the paper. It usually forms the print image by pressing an inked ribbon against the paper using a hammer or pins. Following are some examples of impact printers i.e. dot matrix printer, daisy wheel printer, Line printers, drum printer, chain printer, band printer.

Non-impact Printers

Non-impact printers do not use a striking device to produce characters on the paper because these printers do not hammer against the paper they are much quieter. Following are some non-impacted printers i.e. Ink-jet printers, Laser printer.

Impact vs Non-impact Printers

Impact printer / Dot-matrix printer	Non impact Printer / Laser Printer
1. It prints characters or images by striking print hammer or wheel against an inked ribbon.	1. It prints characters and images without striking the papers.
2. Its speed comparatively slower.	2. Its speed faster.
3. Its printing quality is lower.	3. Its printing quality is higher.
4. It normally uses continuous paper sheet.	4. It normally uses individual paper sheet.
5. It generates noise during printing.	5. It does not generate noise during printing.
6. It uses inked ribbon for printing.	6. It uses toner or cartridge for painting and printing.
7. It is less expensive.	7. It is more expensive.
8. Dot matrix is an impact printer	8. Laser printer is a non-impact printer

Classification of Printer

- Printer classification based on their technology. Typical printer types are:
- **Impact Printer**

1. Daisy-wheel printer
2. Dot matrix printer

- **Non Impact Printer**

3. Ink-jet printer
4. Laser printer

WHEEL PRINTER

1. Printers were initially based on typewriter technology
2. A character shaped piece of metal was moved into contact with an inked ribbon in contact with the paper so that ink is transferred.
3. Development of this technology culminated in the daisy wheel printer, a relatively low cost yet high quality device.
4. Each character is placed on the end of a flexible arm and a complete set arranged around a central hub.
5. This collection spins around and a hammer behind the wheel is triggered at the correct time to force the required character into contact with the ribbon.
6. The flexible arm allows the character to stop momentarily to prevent smearing.
7. The wheel mechanism is placed on a carriage which

Dot Matrix Printer

- A dot matrix printer or impact matrix printer refers to a type of computer printer with a print head that runs back and forth on the page and prints by impact, striking an ink-soaked cloth ribbon against the paper, much like a typewriter. Dot matrix technology uses a series or matrix of pins to create printed dots arranged to form characters on a piece of paper. Because the printing involves mechanical pressure, these printers can create carbon copies and carbonless copies. The print head mechanism pushes each pin into the ribbon, which then strikes the paper.

Dot Matrix Printer

Advantages

1. They can print on multi-part stationary or make carbon copies
2. Low printing cost
3. They can bear environmental conditions.
4. Long life

Disadvantages

1. Noise
2. Low resolution
3. Very limited color performance
4. Low speed

Ink Jet Printers

- An Ink-Jet printer is a type of computer printer that creates a digital image by propelling droplets of ink onto paper. Ink jet printers are the most commonly used type of printer and range from small inexpensive consumer models to very large professional machines that can cost up to thousands of dollars. Its consumable called inkjet cartridge.

Week 17

Printers

What is Piezoelectric effect?

- Crystals, which acquire a charge when compressed, twisted or distorted, are said to be piezoelectric.
- Piezoelectricity is the ability of some materials (notably crystals and certain ceramics) to generate an electric charge in response to applied mechanical stress.
- The piezoelectric effect is reversible in that materials exhibiting the direct piezoelectric effect (the production of electricity when stress is applied) also exhibit the converse piezoelectric effect (the production of stress and/or strain when an electric field is applied). Some crystals will exhibit a maximum shape change of about 0.1% of the original dimension.

Ink Jet Printers

Piezoelectric Ink Jet

- All Epson printers and most commercial and industrial ink jet printers use a piezoelectric material in an ink-filled chamber behind each nozzle instead of a heating element. When a voltage is applied, the crystal changes shape or size, which generates a pressure pulse in the fluid forcing a droplet of ink from the nozzle. This is essentially the same mechanism as the thermal inkjet but generates the pressure pulse using a different physical principle. Piezoelectric ink jet allows a wider variety of inks than thermal or continuous ink jet but is more expensive

Ink Jet Printers

- Conductive ink is forced through a very small nozzle to produce a high speed stream or jet of drops of ink.
- The size and spacing of these drops are made constant by vibrating the nozzle compartment at an ultrasonic frequency with a crystal. Vibrating frequency of crystal: 100KHz. Drop diameter – 0.06mm (0.0025 inch) Drop spacing – 0.15mm (0.006 inch)
- Each drop of ink, after leaving the cavity, is given a charging specific charge as it passes through a electrode located next to the nozzle.
- The drops are deflected vertically by a second electrode structure and strike the paper.
- The horizontal position is normally moving the ink jet system.

Printers

- The amount of deflection is determined by the charge on the drop.
- With no charge there is no deflection and these drops are collected in a gutter placed close to the paper.
- Increasing charge increases deflection so that drops can be placed as desired.
- For high quality printing approx. 1000 drops are required per character. With 105 drops per second release from the nozzle (100KHz vib. rate), 100 characters can be printed per second.

Ink Jet Printers

- **Advantages**

1. Low printer cost
2. Compact/Small size
3. Low noise
4. No warm up time compare to laser printer

- **Disadvantages**

5. The ink is often very expensive (for a typical OEM cartridge cost RM70 for 16ml, RM4375 per liter)
6. Lifetime on inkjet prints produced by inkjet printer is limited. They will eventually fade and the color balance may change.
3. Easy get “blur” if get water drop.
4. Easy to get clogging on inkjet nozzles.
5. Must print it once every few days. Make sure print head won’t dried up.

Laser Printers

- A laser printer works like a photocopy machine. Laser printers produce images on paper by directing a laser beam at a mirror which bounces the beam onto a drum.

- The drum has a special coating on it to which toner (an ink powder) sticks. The drum has a positive charged wire. A laser beam when hits the positively charged drum, it (the drum) becomes neutralized. From all those areas of drum which become neutralized, the toner detaches.
- As the paper rolls by the drum, the toner is transferred to the paper printing the letters or other graphics on the paper. A hot roller bonds the toner to the paper.

Laser Printers

- **Advantages:**

1. The main advantages of Laser printer is its speed & efficiency at which it prints high-quality graphics & text.
2. Laser printers produce high-quality output as compared to other printers.
3. Laser printers are quite and does not produce disturbing sounds.
4. They are also capable to produce color prints

Laser Printers

- **Disadvantages:**

1. The main disadvantages of Laser printer is its cost, they are relatively costly as compared to other printers.
2. The maintenance, repair & servicing charges are also high of these printers.
3. Laser printers emit small amount of ozone are hazardous to health and the atmosphere.